

## Patent Application for

**APPARATUS AND METHODS FOR OUTPUT BUFFER CIRCUITRY WITH  
CONSTANT OUTPUT POWER IN RADIO-FREQUENCY CIRCUITRY**

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**PATENT DOCUMENTS****Cross-Reference to Related Applications**

This patent application is a continuation-in-part of U.S. Patent Application Serial No. 09/821,342, Attorney Docket No. SILA:072, titled "Partitioned Radio-Frequency Apparatus and Associated Methods," and filed on March 29, 2001. Furthermore, this patent application claims priority to Provisional U.S. Patent Application Serial No. 60/261,506, Attorney Docket No. SILA:072PZ1, filed on January 12, 2001; Provisional U.S. Patent Application Serial No. 25 60/273,119, Attorney Docket No. SILA:072PZ2, titled "Partitioned RF Apparatus with Digital Interface and Associated Methods," filed on March 2, 2001; and Provisional U.S. Patent Application Serial No. 60/333,664, Attorney Docket No. SILA:099PZ1, titled "Output Buffer Output Buffer for Local Oscillator and Synthesizer," filed on November 27, 2001.

Furthermore, this patent application incorporates by reference the following patent documents: U.S. Patent Application Serial No. 09/708,339, Attorney Docket No. SILA:035C1, titled “Method and Apparatus for Operating a PLL with a Phase Detector/Sample Hold Circuit for Synthesizing High-Frequency Signals for Wireless Communications,” filed on November 8, 5 2000; U.S. Patent Application Serial No. \_\_\_\_\_, Attorney Docket No. SILA:078, titled “Digital Architecture for Radio-Frequency Apparatus and Associated Methods”; U.S. Patent Application Serial No. \_\_\_\_\_, Attorney Docket No. SILA:097, titled “Notch Filter for DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods”; U.S. Patent Application Serial No. \_\_\_\_\_, Attorney Docket No. SILA:098, titled “DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods”; U.S. Patent Application Serial No. \_\_\_\_\_, Attorney Docket No. SILA:074, titled “Radio-Frequency Communication Apparatus and Associated Methods”; U.S. Patent Application Serial No. \_\_\_\_\_, Attorney Docket No. SILA:075, titled “Apparatus and Methods for Generating Radio Frequencies in Communication Circuitry”; U.S. Patent Application Serial No. 10 \_\_\_\_\_, Attorney Docket No. SILA:096, titled “Apparatus for Generating Multiple Radio Frequencies in Communication Circuitry and Associated Methods”; U.S. Patent Application Serial No. \_\_\_\_\_, Attorney Docket No. SILA:107, titled “Apparatus and Method for Front-End Circuitry in Radio-Frequency Apparatus”; and Provisional U.S. Patent Application Serial No. 60/333,664, Attorney Docket No. SILA:099PZ1, titled “Output Buffer 15 Output Buffer for Local Oscillator and Synthesizer,” filed on November 27, 2001.

## **Technical Field of the Invention**

This invention relates to radio-frequency (RF) apparatus, such as receivers, transmitters, and transceivers. More particularly, the invention concerns output buffer circuitry in RF apparatus.

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## **Background**

The proliferation and popularity of mobile radio and telephony applications has led to market demand for communication systems with low cost, low power, and small form-factor radio-frequency (RF) transceivers. As a result, recent research has focused on providing monolithic transceivers using low-cost complementary metal-oxide semiconductor (CMOS) technology. One aspect of research efforts has focused on providing an RF transceiver within a single integrated circuit (IC). The integration of transceiver circuits is not a trivial problem, as it must take into account the requirements of the transceiver's circuitry and the communication standards governing the transceiver's operation.

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From the perspective of the transceiver's circuitry, RF transceivers typically include sensitive components susceptible to noise and interference with one another and with external sources. Integrating the transceiver's circuitry into one integrated circuit may exacerbate interference among the various blocks of the transceiver's circuitry. Moreover, communication standards governing RF transceiver operation outline a set of requirements for noise, inter-modulation, blocking performance, output power, and spectral emission of the transceiver. Unfortunately, no technique for addressing all of the above issues in high-performance RF

receivers or transceivers, for example, RF transceivers used in cellular and telephony applications, has been developed. A need therefore exists for techniques of partitioning and integrating RF receivers or transceivers that would provide low-cost, low form-factor RF transceivers for high-performance applications, for example, in cellular handsets.

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A further aspect of RF apparatus, such as RF transceivers, receivers, and transmitters, relates to providing local oscillator (LO) signals. Typical RF apparatus employ LO circuitry that generates and supplies LO signals. The RF apparatus use LO signals in the receive-path circuitry and/or in the transmit-path circuitry. Consequently, the stability of the LO signal impacts the performance of the RF apparatus. Conventional LO circuitry suffer from variations in the output power of the LO output signals. The variations result, for example, from semiconductor manufacturing process variations and temperature changes. Regardless of the source, the variations in the output power of the LO output signals degrades the performance of the LO circuitry and, consequently, the performance of the RF circuitry. A need therefore exists for LO circuitry that provides a relatively constant output power over physical variations, such as process and temperature variations.

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## **Summary of the Invention**

This invention relates to output buffer circuitry for use in various RF apparatus. Output buffer circuitries according to the invention solve the problem of providing LO circuitries that provide substantially constant output power over physical variations, such as process and  
5 temperature variations.

One aspect of the invention concerns apparatus for providing a substantially constant output power. In one embodiment, a buffer circuitry buffers a radio-frequency (RF) signal. The buffer circuitry includes a complementary pair of switches and a power source. The a complementary pair of switches has an input terminal and output terminal. The input terminal of the complementary pair of switches responds to the RF signal. The output terminal of the complementary pair of switches couples to an output of the buffer circuitry. The power source includes a capacitor coupled to a current source. The power source couples to the complementary pair of switches. The power source supplies power to the complementary pair of  
15 switches in a manner that the buffer circuitry supplies a substantially constant power level at its output.

## **Description of the Drawings**

The appended drawings illustrate only exemplary embodiments of the invention and  
20 therefore should not be considered as limiting its scope. The disclosed inventive concepts lend themselves to other equally effective embodiments. In the drawings, the same numeral

designators used in more than one drawing denote the same, similar, or equivalent functionality, components, or blocks.

FIG. 1 illustrates the block diagram of an RF transceiver that includes radio circuitry that  
5 operates in conjunction with a baseband processor circuitry.

FIG. 2A shows RF transceiver circuitry partitioned according to the invention.

FIG. 2B depicts another embodiment of RF transceiver circuitry partitioned according to

10 the invention, in which the reference generator circuitry resides within the same circuit partition,  
or circuit block, as does the receiver digital circuitry.

FIG. 2C illustrates yet another embodiment of RF transceiver circuitry partitioned

according to invention, in which the reference generator circuitry resides within the baseband  
15 processor circuitry.

FIG. 2D shows another embodiment of RF transceiver circuitry partitioned according to

the invention, in which the receiver digital circuitry resides within the baseband processor  
circuitry.

FIG. 3 illustrates interference mechanisms among the various blocks of an RF transceiver, which the embodiments of the invention in FIGS. 2A-2D, depicting RF transceivers partitioned according to the invention, seek to overcome, reduce, or minimize.

5 FIG. 4 shows a more detailed block diagram of RF transceiver circuitry partitioned according to the invention.

10 FIG. 5 illustrates an alternative technique for partitioning RF transceiver circuitry.

15 FIG. 6 shows yet another alternative technique for partitioning RF transceiver circuitry.

FIG. 7 depicts a more detailed block diagram of RF transceiver circuitry partitioned according to the invention, in which the receiver digital circuitry resides within the baseband processor circuitry.

15 FIG. 8 illustrates a more detailed block diagram of a multi-band RF transceiver circuitry partitioned according to the invention.

20 FIG. 9A shows a block diagram of an embodiment of the interface between the receiver digital circuitry and receiver analog circuitry in an RF transceiver according to the invention.

FIG. 9B depicts a block diagram of another embodiment of the interface between the baseband processor circuitry and the receiver analog circuitry in an RF transceiver according to the invention, in which the receiver digital circuitry resides within the baseband processor circuitry.

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FIG. 10 illustrates a more detailed block diagram of the interface between the receiver analog circuitry and the receiver digital circuitry, with the interface configured as a serial interface.

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FIG. 11A shows a more detailed block diagram of an embodiment of the interface between the receiver analog circuitry and the receiver digital circuitry, with the interface configured as a data and clock signal interface.

15 FIG. 11B illustrates a block diagram of an embodiment of a delay-cell circuitry that includes a clock driver circuitry in tandem with a clock receiver circuitry.

FIG. 12 depicts a schematic diagram of an embodiment of a signal-driver circuitry used to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.

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FIGS. 13A and 13B illustrate schematic diagrams of embodiments of signal-receiver circuitries used to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.

5 FIG. 14 shows a schematic diagram of another signal-driver circuitry that one may use to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.

10 FIG. 15 depicts a portion of a prior-art local-oscillator circuitry that includes an output buffer circuitry.

15 FIG. 16 illustrates an embodiment of the output circuitry of an LO circuitry according to invention that helps to reduce variations in the output power of the LO circuitry

FIG. 17 shows another embodiment of an output buffer circuitry according to the  
15 invention.

20 FIG. 18 depicts a further embodiment of an output buffer circuitry according to the invention.

FIGS. 19A-19B illustrate equivalent circuits that represent a portion of an output buffer circuitry according to the invention during different states of its operation.

10 FIG. 19C depicts waveforms that correspond to various signals in one embodiment of the

invention.

15 FIG. 20 illustrates an embodiment of an output buffer circuitry according to the invention

that can buffer outputs of more than VCO circuitry.

20 FIG. 21 shows an embodiment according to the invention for an output buffer circuitry

that provides a differential output signal from a differential input signal.

25 FIG. 22 depicts an embodiment of an output buffer circuitry according to the invention

that has programmable or adjustable output power level.

30 FIG. 23 illustrates an adjustable current source for use in exemplary embodiments

according to the invention.

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FIG. 24 shows a block diagram of an embodiment of an output buffer circuitry according

to the invention.

40 FIG. 25 depicts more details of the circuit arrangement within the embodiment shown in

20 FIG. 24.

FIG. 26A illustrates an embodiment of an LO circuitry that uses an output buffer circuitry according to the invention.

FIG. 26B shows a second embodiment of an LO circuitry that uses an output buffer circuitry according to the invention.

FIG. 26C depicts a third embodiment of an LO circuitry that uses an output buffer circuitry according to the invention.

## 10 **Detailed Description**

This invention in part contemplates partitioning RF apparatus so as to provide highly integrated, high-performance, low-cost, and low form-factor RF solutions. One may use RF apparatus according to the invention in high-performance communication systems. More particularly, the invention in part relates to partitioning RF receiver or transceiver circuitry in a way that minimizes, reduces, or overcomes interference effects among the various blocks of the RF receiver or transceiver, while simultaneously satisfying the requirements of the standards that govern RF receiver or transceiver performance. Those standards include the Global System for Mobile (GSM) communication, Personal Communication Services (PCS), Digital Cellular System (DCS), Enhanced Data for GSM Evolution (EDGE), and General Packet Radio Services (GPRS). RF receiver or transceiver circuitry partitioned according to the invention therefore overcomes interference effects that would be present in highly integrated RF receivers or transceivers while meeting the requirements of the governing standards at low cost and with a

low form-factor. The description of the invention refers to circuit partition and circuit block interchangeably.

FIG. 1 shows the general block diagram of an RF transceiver circuitry 100 according to  
5 the invention. The RF transceiver circuitry 100 includes radio circuitry 110 that couples to an antenna 130 via a bi-directional signal path 160. The radio circuitry 110 provides an RF transmit signal to the antenna 130 via the bi-directional signal path 160 when the transceiver is in transmit mode. When in the receive mode, the radio circuitry 110 receives an RF signal from the antenna 130 via the bi-directional signal path 160.

10 The radio circuitry 110 also couples to a baseband processor circuitry 120. The baseband processor circuitry 120 may comprise a digital-signal processor (DSP). Alternatively, or in addition to the DSP, the baseband processor circuitry 120 may comprise other types of signal processor, as persons skilled in the art understand. The radio circuitry 110 processes the RF  
15 signals received from the antenna 130 and provides receive signals 140 to the baseband processor circuitry 120. In addition, the radio circuitry 110 accepts transmit input signals 150 from the baseband processor 120 and provides the RF transmit signals to the antenna 130.

FIGS. 2A-2D show various embodiments of RF transceiver circuitry partitioned  
20 according to the invention. FIG. 3 and its accompanying description below make clear the considerations that lead to the partitioning of the RF transceiver circuitry as shown in FIGS. 2A-  
2D. FIG. 2A illustrates an embodiment 200A of an RF transceiver circuitry partitioned

according to the invention. In addition to the elements described in connection with FIG. 1, the RF transceiver 200A includes antenna interface circuitry 202, receiver circuitry 210, transmitter circuitry 216, reference generator circuitry 218, and local oscillator circuitry 222.

5 The reference generator circuitry 218 produces a reference signal 220 and provides that

signal to the local oscillator circuitry 222 and to receiver digital circuitry 212. The reference signal 220 preferably comprises a clock signal, although it may include other signals, as desired.

The local oscillator circuitry 222 produces an RF local oscillator signal 224, which it provides to

receiver analog circuitry 208 and to the transmitter circuitry 216. The local oscillator circuitry

10 222 also produces a transmitter intermediate-frequency (IF) local oscillator signal 226 and

provides that signal to the transmitter circuitry 216. Note that, in RF transceivers according to

the invention, the receiver analog circuitry 208 generally comprises mostly analog circuitry in

addition to some digital or mixed-mode circuitry, for example, analog-to-digital converter (ADC)

circuitry and circuitry to provide an interface between the receiver analog circuitry and the

15 receiver digital circuitry, as described below.

The antenna interface circuitry 202 facilitates communication between the antenna 130

and the rest of the RF transceiver. Although not shown explicitly, the antenna interface circuitry

20 202 may include a transmit/receive mode switch, RF filters, and other transceiver front-end

circuitry, as persons skilled in the art understand. In the receive mode, the antenna interface

circuitry 202 provides RF receive signals 204 to the receiver analog circuitry 208. The receiver

analog circuitry 208 uses the RF local oscillator signal 224 to process (*e.g.*, down-convert) the

RF receive signals 204 and produce a processed analog signal. The receiver analog circuitry 208 converts the processed analog signal to digital format and supplies the resulting digital receive signals 228 to the receiver digital circuitry 212. The receiver digital circuitry 212 further processes the digital receive signals 228 and provides the resulting receive signals 140 to the

5 baseband processor circuitry 120.

In the transmit mode, the baseband processor circuitry 120 provides transmit input signals  
150 to the transmitter circuitry 216. The transmitter circuitry 216 uses the RF local oscillator  
signal 224 and the transmitter IF local oscillator signal 226 to process the transmit input signals  
10 150 and to provide the resulting transmit RF signal 206 to the antenna interface circuitry 202.  
The antenna interface circuitry 202 may process the transmit RF signal further, as desired, and  
provide the resulting signal to the antenna 130 for propagation into a transmission medium.

The embodiment 200A in FIG. 2A comprises a first circuit partition, or circuit block, 214  
15 that includes the receiver analog circuitry 208 and the transmitter circuitry 216. The embodiment  
200A also includes a second circuit partition, or circuit block, that includes the receiver digital  
circuitry 212. The embodiment 200A further includes a third circuit partition, or circuit block,  
that comprises the local oscillator circuitry 222. The first circuit partition 214, the second circuit  
partition 212, and the third circuit partition 222 are partitioned from one another so that  
20 interference effects among the circuit partitions tend to be reduced. The first, second, and third  
circuit partitions preferably each reside within an integrated circuit device. In other words,  
preferably the receiver analog circuitry 208 and the transmitter circuitry 216 reside within an

integrated circuit device, the receiver digital circuitry 212 resides within another integrated circuit device, and the local oscillator circuitry 222 resides within a third integrated circuit device.

5 FIG. 2B shows an embodiment 200B of an RF transceiver circuitry partitioned according to the invention. The embodiment 200B has the same circuit topology as that of embodiment 200A in FIG. 2A. The partitioning of embodiment 200B, however, differs from the partitioning  
10 of embodiment 200A. Like embodiment 200A, embodiment 200B has three circuit partitions, or circuit blocks. The first and the third circuit partitions in embodiment 200B are similar to the  
15 first and third circuit partitions in embodiment 200A. The second circuit partition 230 in embodiment 200B, however, includes the reference signal generator 218 in addition to the receiver digital circuitry 212. As in embodiment 200A, embodiment 200B is partitioned so that interference effects among the three circuit partitions tend to be reduced.

15 FIG. 2C illustrates an embodiment 200C, which constitutes a variation of embodiment 200A in FIG. 2A. Embodiment 200C shows that one may place the reference signal generator 218 within the baseband processor circuitry 120, as desired. Placing the reference signal generator 218 within the baseband processor circuitry 120 obviates the need for either discrete  
20 reference signal generator circuitry 218 or an additional integrated circuit or module that includes the reference signal generator 218. Embodiment 200C has the same partitioning as embodiment 200A, and operates in a similar manner.

Note that FIGS. 2A-2C show the receiver circuitry 210 as a block to facilitate the description of the embodiments shown in those figures. In other words, the block containing the receiver circuitry 210 in FIGS. 2A-2C constitutes a conceptual depiction of the receiver circuitry within the RF transceiver shown in FIGS. 2A-2C, not a circuit partition or circuit block.

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FIG. 2D shows an embodiment 200D of an RF transceiver partitioned according to the invention. The RF transceiver in FIG. 2D operates similarly to the transceiver shown in FIG.

2A. The embodiment 200D, however, accomplishes additional economy by including the receiver digital circuitry 212 within the baseband processor circuitry 120. As one alternative, one may integrate the entire receiver digital circuitry 212 on the same integrated circuit device that includes the baseband processor circuitry 120. Note that one may use software (or firmware), hardware, or a combination of software (or firmware) and hardware to realize the functions of the receiver digital circuitry 212 within the baseband processor circuitry 120, as persons skilled in the art who have the benefit of the description of the invention understand.

15 Note also that, similar to the embodiment 200C in FIG. 2C, the baseband processor circuitry 120 in embodiment 200D may also include the reference signal generator 218, as desired.

The partitioning of embodiment 200D involves two circuit partitions, or circuit blocks.

The first circuit partition 214 includes the receiver analog circuitry 208 and the transmitter circuitry 216. The second circuit partition includes the local oscillator circuitry 222. The first and second circuit partitions are partitioned so that interference effects between them tend to be reduced.

FIG. 3 shows the mechanisms that may lead to interference among the various blocks or components in a typical RF transceiver, for example, the transceiver shown in FIG. 2A. Note that the paths with arrows in FIG. 3 represent interference mechanisms among the blocks within the transceiver, rather than desired signal paths. One interference mechanism results from the reference signal 220 (see FIGS. 2A-2D), which preferably comprises a clock signal. In the preferred embodiments, the reference generator circuitry produces a clock signal that may have a frequency of 13 MHz (GSM clock frequency) or 26 MHz. If the reference generator produces a 26 MHz clock signal, RF transceivers according to the invention preferably divide that signal by two to produce a 13 MHz master system clock. The clock signal typically includes voltage pulses that have many Fourier series harmonics. The Fourier series harmonics extend to many multiples of the clock signal frequency. Those harmonics may interfere with the receiver analog circuitry 208 (e.g., the low-noise amplifier, or LNA), the local oscillator circuitry 222 (e.g., the synthesizer circuitry), and the transmitter circuitry 216 (e.g., the transmitter's voltage-controlled oscillator, or VCO). FIG. 3 shows these sources of interference as interference mechanisms 360, 350, and 340.

The receiver digital circuitry 212 uses the output of the reference generator circuitry 218, which preferably comprises a clock signal. Interference mechanism 310 exists because of the sensitivity of the receiver analog circuitry 208 to the digital switching noise and harmonics present in the receiver digital circuitry 212. Interference mechanism 310 may also exist because of the digital signals (for example, clock signals) that the receiver digital circuitry 212

communicates to the receiver analog circuitry 208. Similarly, the digital switching noise and harmonics in the receiver digital circuitry 212 may interfere with the local oscillator circuitry 222, giving rise to interference mechanism 320 in FIG. 3.

5           The local oscillator circuitry 222 typically uses an inductor in an inductive-capacitive (LC) resonance tank (not shown explicitly in the figures). The resonance tank may circulate relatively large currents. Those currents may couple to the sensitive circuitry within the transmitter circuitry 216 (e.g., the transmitter's VCO), thus giving rise to interference mechanism 330. Similarly, the relatively large currents circulating within the resonance tank of the local 10 oscillator circuitry 222 may saturate sensitive components within the receiver analog circuitry 208 (e.g., the LNA circuitry). FIG. 3 depicts this interference source as interference mechanism 370.

15           The timing of the transmit mode and receive mode in the GSM specifications help to mitigate potential interference between the transceiver's receive-path circuitry and its transmit-path circuitry. The GSM specifications use time-division duplexing (TDD). According to the TDD protocol, the transceiver deactivates the transmit-path circuitry while in the receive mode of operation, and vice-versa. Consequently, FIG. 3 does not show potential interference mechanisms between the transmitter circuitry 216 and either the receiver digital circuitry 212 or 20 the receiver analog circuitry 208.

As FIG. 3 illustrates, interference mechanisms exist between the local oscillator circuitry 222 and each of the other blocks or components in the RF transceiver. Thus, to reduce interference effects, RF transceivers according to the invention preferably partition the local oscillator circuitry 222 separately from the other transceiver blocks shown in FIG. 3. Note,

5 however, that in some circumstances one may include parts or all of the local oscillator circuitry within the same circuit partition (for example, circuit partition 214 in FIGS. 2A-2D) that includes the receiver analog circuitry and the transmitter circuitry, as desired. Typically, a voltage-

controlled oscillator (VCO) within the local oscillator circuitry causes interference with other

10 sensitive circuit blocks (for example, the receiver analog circuitry) through undesired coupling mechanisms. If those coupling mechanisms can be mitigated to the extent that the performance

15 characteristics of the RF transceiver are acceptable in a given application, then one may include the local oscillator circuitry within the same circuit partition as the receiver analog circuitry and the transmitter circuitry. Alternatively, if the VCO circuitry causes unacceptable levels of interference, one may include other parts of the local oscillator circuitry within the circuit

partition that includes the receiver analog circuitry and the transmitter circuitry, but exclude the

VCO circuitry from that circuit partition.

To reduce the effects of interference mechanism 310, RF transceivers according to the

invention partition the receiver analog circuitry 208 separately from the receiver digital circuitry

20 212. Because of the mutually exclusive operation of the transmitter circuitry 216 and the receiver analog circuitry 208 according to GSM specifications, the transmitter circuitry 216 and the receiver analog circuitry 208 may reside within the same circuit partition, or circuit block.

Placing the transmitter circuitry 216 and the receiver analog circuitry 208 within the same circuit partition results in a more integrated RF transceiver overall. The RF transceivers shown in FIGS. 2A-2D employ partitioning techniques that take advantage of the above analysis of the interference mechanisms among the various transceiver components. To reduce interference effects among the various circuit partitions or circuit blocks even further, RF transceivers according to the invention also use differential signals to couple the circuit partitions or circuit blocks to one another.

FIG. 4 shows a more detailed block diagram of an embodiment 400 of an RF transceiver

partitioned according to the invention. The transceiver includes receiver analog circuitry 408, receiver digital circuitry 426, and transmitter circuitry 465. In the receive mode, the antenna interface circuitry 202 provides an RF signal 401 to a filter circuitry 403. The filter circuitry 403 provides a filtered RF signal 406 to the receiver analog circuitry 408. The receiver analog circuitry 408 includes down-converter (*i.e.*, mixer) circuitry 409 and analog-to-digital converter (ADC) circuitry 418. The down-converter circuitry 409 mixes the filtered RF signal 406 with an RF local oscillator signal 454, received from the local oscillator circuitry 222. The down-converter circuitry 409 provides an in-phase analog down-converted signal 412 (*i.e.*, *I*-channel signal) and a quadrature analog down-converted signal 415 (*i.e.*, *Q*-channel signal) to the ADC circuitry 418.

The ADC circuitry 418 converts the in-phase analog down-converted signal 412 and the quadrature analog down-converted signal 415 into a one-bit in-phase digital receive signal 421

and a one-bit quadrature digital receive signal 424. (Note that FIGS. 4-8 illustrate signal flow, rather than specific circuit implementations; for more details of the circuit implementation, for example, more details of the circuitry relating to the one-bit in-phase digital receive signal 421 and the one-bit quadrature digital receive signal 424, see FIGS. 9-14.) Thus, The ADC circuitry

5      418 provides the one-bit in-phase digital receive signal 421 and the one-bit quadrature digital receive signal 424 to the receiver digital circuitry 426. As described below, rather than, or in addition to, providing the one-bit in-phase and quadrature digital receive signals to the receiver  
digital circuitry 426, the digital interface between the receiver analog circuitry 408 and the receiver digital circuitry 426 may communicate various other signals. By way of illustration,  
10     those signals may include reference signals (e.g., clock signals), control signals, logic signals, hand-shaking signals, data signals, status signals, information signals, flag signals, and/or configuration signals. Moreover, the signals may constitute single-ended or differential signals, as desired. Thus, the interface provides a flexible communication mechanism between the receiver analog circuitry and the receiver digital circuitry.

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The receiver digital circuitry 426 includes digital down-converter circuitry 427, digital

filter circuitry 436, and digital-to-analog converter (DAC) circuitry 445. The digital down-

converter circuitry 427 accepts the one-bit in-phase digital receive signal 421 and the one-bit

quadrature digital receive signal 424 from the receiver analog circuitry 408. The digital down-

20     converter circuitry 427 converts the received signals into a down-converted in-phase signal 430

and a down-converted quadrature signal 433 and provides those signals to the digital filter

circuitry 436. The digital filter circuitry 436 preferably comprises an infinite impulse response

(IIR) channel-select filter that performs various filtering operations on its input signals. The digital filter circuitry 436 preferably has programmable response characteristics. Note that, rather than using an IIR filter, one may use other types of filter (e.g., finite impulse-response, or FIR, filters) that provide fixed or programmable response characteristics, as desired.

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The digital filter circuitry 436 provides a digital in-phase filtered signal 439 and a digital quadrature filtered signal 442 to the DAC circuitry 445. The DAC circuitry 445 converts the digital in-phase filtered signal 439 and the digital quadrature filtered signal 442 to an in-phase analog receive signal 448 and a quadrature analog receive signal 451, respectively. The baseband processor circuitry 120 accepts the in-phase analog receive signal 448 and the quadrature analog receive signal 451 for further processing.

The transmitter circuitry 465 comprises baseband up-converter circuitry 466, offset phase-lock-loop (PLL) circuitry 472, and transmit voltage-controlled oscillator (VCO) circuitry

15 481. The transmit VCO circuitry 481 typically has low-noise circuitry and is sensitive to external noise. For example, it may pick up interference from digital switching because of the high gain that results from the resonant LC-tank circuit within the transmit VCO circuitry 481.

The baseband up-converter circuitry 466 accepts an intermediate frequency (IF) local oscillator signal 457 from the local oscillator circuitry 222. The baseband up-converter circuitry 466 mixes 20 the IF local oscillator signal 457 with an analog in-phase transmit input signal 460 and an analog quadrature transmit input signal 463 and provides an up-converted IF signal 469 to the offset PLL circuitry 472.

The offset PLL circuitry 472 effectively filters the IF signal 469. In other words, the offset PLL circuitry 472 passes through it signals within its bandwidth but attenuates other signals. In this manner, the offset PLL circuitry 472 attenuates any spurious or noise signals outside its bandwidth, thus reducing the requirement for filtering at the antenna 130, and reducing system cost, insertion loss, and power consumption. The offset PLL circuitry 472 forms a feedback loop with the transmit VCO circuitry 481 via an offset PLL output signal 475 and a transmit VCO output signal 478. The transmit VCO circuitry 481 preferably has a constant-amplitude output signal.

The offset PLL circuitry 472 uses a mixer (not shown explicitly in FIG. 4) to mix the RF local oscillator signal 454 with the transmit VCO output signal 478. Power amplifier circuitry 487 accepts the transmit VCO output signal 478, and provides an amplified RF signal 490 to the antenna interface circuitry 202. The antenna interface circuitry 202 and the antenna 130 operate

as described above. RF transceivers according to the invention preferably use transmitter circuitry 465 that comprises analog circuitry, as shown in FIG. 4. Using such circuitry minimizes interference with the transmit VCO circuitry 481 and helps to meet emission specifications for the transmitter circuitry 465.

The receiver digital circuitry 426 also accepts the reference signal 220 from the reference generator circuitry 218. The reference signal 220 preferably comprises a clock signal. The receiver digital circuitry 426 provides to the transmitter circuitry 465 a switched reference signal

494 by using a switch 492. Thus, the switch 492 may selectively provide the reference signal 220 to the transmitter circuitry 465. Before the RF transceiver enters its transmit mode, the receiver digital circuitry 426 causes the switch 492 to close, thus providing the switched reference signal 494 to the transmitter circuitry 465.

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The transmitter circuitry 465 uses the switched reference signal 494 to calibrate or adjust some of its components. For example, the transmitter circuitry 465 may use the switched reference signal 494 to calibrate some of its components, such as the transmit VCO circuitry 481, for example, as described in commonly owned U.S. Patent Number 6,137,372, incorporated by reference here in its entirety. The transmitter circuitry 465 may also use the switched reference signal 494 to adjust a voltage regulator within its output circuitry so as to transmit at known levels of RF radiation or power.

While the transmitter circuitry 465 calibrates and adjusts its components, the analog

15      circuitry within the transmitter circuitry 465 powers up and begins to settle. When the transmitter circuitry 465 has finished calibrating its internal circuitry, the receiver digital circuitry 426 causes the switch 492 to open, thus inhibiting the supply of the reference signal 220 to the transmitter circuitry 465. At this point, the transmitter circuitry may power up the power amplifier circuitry 487 within the transmitter circuitry 465. The RF transceiver subsequently  
20      enters the transmit mode of operation and proceeds to transmit.

Note that FIG. 4 depicts the switch 492 as a simple switch for conceptual, schematic purposes. One may use a variety of devices to realize the function of the controlled switch 492, for example, semiconductor switches, gates, or the like, as persons skilled in the art who have the benefit of the disclosure of the invention understand. Note also that, although FIG. 4 shows the 5 switch 492 as residing within the receiver digital circuitry 426, one may locate the switch in other locations, as desired. Placing the switch 492 within the receiver digital circuitry 426 helps to confine to the receiver digital circuitry 426 the harmonics that result from the switching circuitry.

10 The embodiment 400 in FIG. 4 comprises a first circuit partition 407, or circuit block,

that includes the receiver analog circuitry 408 and the transmitter circuitry 465. The embodiment

400 also includes a second circuit partition, or circuit block, that includes the receiver digital

circuitry 426. Finally, the embodiment 400 includes a third circuit partition, or circuit block, that

comprises the local oscillator circuitry 222. The first circuit partition 407, the second circuit

15 partition, and the third circuit partition are partitioned from one another so that interference

effects among the circuit partitions tend to be reduced. That arrangement tends to reduce the

interference effects among the circuit partitions by relying on the analysis of interference effects

provided above in connection with FIG. 3. Preferably, the first, second, and third circuit

partitions each reside within an integrated circuit device. To further reduce interference effects

20 among the circuit partitions, the embodiment 400 in FIG. 4 uses differential signals wherever

possible. The notation “(diff.)” adjacent to signal lines or reference numerals in FIG. 4 denotes

the use of differential lines to propagate the annotated signals.

Note that the embodiment 400 shown in FIG. 4 uses an analog-digital-analog signal path in its receiver section. In other words, the ADC circuitry 418 converts analog signals into digital signals for further processing, and later conversion back into analog signals by the DAC circuitry

5 445. RF transceivers according to the invention use this particular signal path for the following reasons. First, the ADC circuitry 418 obviates the need for propagating signals from the receiver analog circuitry 408 to the receiver digital circuitry 426 over an analog interface with a relatively high dynamic range. The digital interface comprising the one-bit in-phase digital receive signal 421 and the one-bit quadrature digital receive signal 424 is less susceptible to the effects of noise  
10 and interference than would be an analog interface with a relatively high dynamic range.

Second, the RF transceiver in FIG. 4 uses the DAC circuitry 445 to maintain compatibility with interfaces commonly used to communicate with baseband processor circuitry in RF transceivers. According to those interfaces, the baseband processor accepts analog, rather

15 than digital, signals from the receive path circuitry within the RF transceiver. In an RF transceiver that meets the specifications of those interfaces, the receiver digital circuitry 426 would provide analog signals to the baseband processor circuitry 120. The receiver digital circuitry 426 uses the DAC circuitry 445 to provide analog signals (*i.e.*, the in-phase analog receive signal 448 and the quadrature analog receive signal 451) to the baseband processor circuitry 120. The DAC circuitry 445 allows programming the common-mode level and the full-scale voltage, which may vary among different baseband processor circuitries.

Third, compared to an analog solution, the analog-digital-analog signal path may result in reduced circuit size and area (for example, the area occupied within an integrated circuit device), thus lower cost. Fourth, the digital circuitry provides better repeatability, relative ease of testing, and more robust operation than its analog counterpart. Fifth, the digital circuitry has less  
5 dependence on supply voltage variation, temperature changes, and the like, than does comparable analog circuitry.

Sixth, the baseband processor circuitry 120 typically includes programmable digital

circuitry, and may subsume the functionality of the digital circuitry within the receiver digital

10 circuitry 426, if desired. Seventh, the digital circuitry allows more precise signal processing, for

example, filtering, of signals within the receive path. Eighth, the digital circuitry allows more

power-efficient signal processing. Finally, the digital circuitry allows the use of readily

programmable DAC circuitry and PGA circuitry that provide for more flexible processing of the

signals within the receive path. To benefit from the analog-digital-analog signal path, RF

15 transceivers according to the invention use a low-IF signal (for example, 100 KHz for GSM

applications) in their receive path circuitry, as using higher IF frequencies may lead to higher

performance demands on the ADC and DAC circuitry within that path. The low-IF architecture

also eases image-rejection requirements, and allows on-chip integration of the digital filter

circuitry 436. Moreover, RF transceivers according to the invention use the digital down-

20 converter circuitry 427 and the digital filter circuitry 436 to implement a digital-IF path in the

receive signal path. The digital-IF architecture facilitates the implementation of the digital

interface between the receiver digital circuitry 426 and the receiver analog circuitry 408.

If the receiver digital circuitry 426 need not be compatible with the common analog

interface to baseband processors, one may remove the DAC circuitry 445 and use a digital

interface to the baseband processor circuitry 120, as desired. In fact, similar to the RF

5 transceiver shown in FIG. 2D, one may realize the function of the receiver digital circuitry 426

within the baseband processor circuitry 120, using hardware, software, or a combination of

hardware and software. In that case, the RF transceiver would include two circuit partitions, or

circuit blocks. The first circuit partition, or circuit block, 407 would include the receiver analog

10 circuitry 408 and the transmitter circuitry 465. A second circuit partition, or circuit block, would

comprise the local oscillator circuitry 222. Note also that, similar to the RF transceiver shown in

FIG. 2C, one may include within the baseband processor circuitry 120 the functionality of the

reference generator circuitry 218, as desired.

One may partition the RF transceiver shown in FIG. 4 in other ways. FIGS. 5 and 6

15 illustrate alternative partitioning of the RF transceiver of FIG. 4. FIG. 5 shows an embodiment

500 of an RF transceiver that includes three circuit partitions, or circuit blocks. A first circuit

partition includes the receiver analog circuitry 408. A second circuit partition 505 includes the

receiver digital circuitry 426 and the transmitter circuitry 465. As noted above, the GSM

specifications provide for alternate operation of RF transceivers in receive and transmit modes.

20 The partitioning shown in FIG. 5 takes advantage of the GSM specifications by including the

receiver digital circuitry 426 and the transmitter circuitry 465 within the second circuit partition

505. A third circuit partition includes the local oscillator circuitry 222. Preferably, the first,

second, and third circuit partitions each reside within an integrated circuit device. Similar to embodiment 400 in FIG. 4, the embodiment 500 in FIG. 5 uses differential signals wherever possible to further reduce interference effects among the circuit partitions.

5 FIG. 6 shows another alternative partitioning of an RF transceiver. FIG. 6 shows an

embodiment 600 of an RF transceiver that includes three circuit partitions, or circuit blocks. A first circuit partition 610 includes part of the receiver analog circuitry, *i.e.*, the down-converter

circuitry 409, together with the transmitter circuitry 465. A second circuit partition 620 includes the ADC circuitry 418, together with the receiver digital circuitry, *i.e.*, the digital down-converter

10 circuitry 427, the digital filter circuitry 436, and the DAC circuitry 445. A third circuit partition

15 includes the local oscillator circuitry 222. Preferably, the first, second, and third circuit partitions

each reside within an integrated circuit device. Similar to embodiment 400 in FIG. 4, the embodiment 600 in FIG. 6 uses differential signals wherever possible to further reduce

interference effects among the circuit partitions.

15

FIG. 7 shows a variation of the RF transceiver shown in FIG. 4. FIG. 7 illustrates an

embodiment 700 of an RF transceiver partitioned according to the invention. Note that, for the

sake of clarity, FIG. 7 does not explicitly show the details of the receiver analog circuitry 408,

the transmitter circuitry 465, and the receiver digital circuitry 426. The receiver analog circuitry

20 408, the transmitter circuitry 465, and the receiver digital circuitry 426 include circuitry similar

to those shown in their corresponding counterparts in FIG. 4. Similar to the RF transceiver

shown in FIG. 2D, the embodiment 700 in FIG. 7 shows an RF transceiver in which the

baseband processor 120 includes the function of the receiver digital circuitry 426. The baseband processor circuitry 120 may realize the function of the receiver digital circuitry 426 using hardware, software, or a combination of hardware and software.

5 Because the embodiment 700 includes the function of the receiver digital circuitry 426

within the baseband processor circuitry 120, it includes two circuit partitions, or circuit blocks.

A first circuit partition 710 includes the receiver analog circuitry 408 and the transmitter circuitry

465. A second circuit partition comprises the local oscillator circuitry 222. Note also that,

similar to the RF transceiver shown in FIG. 2C, one may also include within the baseband

10 processor circuitry 120 the functionality of the reference generator circuitry 218, as desired.

FIG. 8 shows an embodiment 800 of a multi-band RF transceiver, partitioned according

15 to the invention. Preferably, the RF transceiver in FIG. 8 operates within the GSM (925 to 960

MHz for reception and 880-915 MHz for transmission), PCS (1930 to 1990 MHz for reception

and 1850-1910 MHz for transmission), and DCS (1805 to 1880 MHz for reception and 1710-

1785 MHz for transmission) bands. Like the RF transceiver in FIG. 4, the RF transceiver in FIG.

19 8 uses a low-IF architecture. The embodiment 800 includes receiver analog circuitry 839,

receiver digital circuitry 851, transmitter circuitry 877, local oscillator circuitry 222, and

reference generator circuitry 218. The local oscillator circuitry 222 includes RF phase-lock loop

20 (PLL) circuitry 840 and intermediate-frequency (IF) PLL circuitry 843. The RF PLL circuitry

840 produces the RF local oscillator, or RF LO, signal 454, whereas the IF PLL circuitry 843

produces the IF local oscillator, or IF LO, signal 457.

Table 1 below shows the preferred frequencies for the RF local oscillator signal 454 during the receive mode:

Band	RF Local Oscillator Frequency (MHz)
GSM	1849.8-1919.8
DCS	1804.9-1879.9
PCS	1929.9-1989.9
All Bands	1804.9-1989.9

Table 1

Table 2 below lists the preferred frequencies for the RF local oscillator signal 454 during the transmit mode:

Band	RF Local Oscillator Frequency (MHz)
GSM	1279-1314
DCS	1327-1402
PCS	1423-1483
All Bands	1279-1483

Table 2

During the receive mode, the IF local oscillator signal 457 is preferably turned off. In preferred embodiments, during the transmit mode, the IF local oscillator signal 457 preferably

has a frequency between 383 MHz and 427 MHz. Note, however, that one may use other frequencies for the RF and IF local oscillator signals 454 and 457, as desired.

The reference generator 218 provides a reference signal 220 that preferably comprises a  
5 clock signal, although one may use other signals, as persons skilled in the art who have the benefit of the description of the invention understand. Moreover, the transmitter circuitry 877 preferably uses high-side injection for the GSM band and low-side injection for the DCS and PCS bands.

10 The receive path circuitry operates as follows. Filter circuitry 812 accepts a GSM RF signal 803, a DCS RF signal 806, and a PCS RF signal 809 from the antenna interface circuitry 202. The filter circuitry 812 preferably contains a surface-acoustic-wave (SAW) filter for each 15 of the three bands, although one may use other types and numbers of filters, as desired. The filter circuitry 812 provides a filtered GSM RF signal 815, a filtered DCS RF signal 818, and a filtered PCS RF signal 821 to low-noise amplifier (LNA) circuitry 824. The LNA circuitry 824 preferably has programmable gain, and in part provides for programmable gain in the receive path circuitry.

20 The LNA circuitry 824 provides an amplified RF signal 827 to down-converter circuitry 409. In exemplary embodiments according to the invention, amplified RF signal 827 includes multiple signal lines, which may be differential signal lines, to accommodate the GSM, DCS, and PCS bands. Note that, rather than using the LNA circuitry with a real output, one may use

an LNA circuitry that has complex outputs (in-phase and quadrature outputs), together with a poly-phase filter circuitry. The combination of the complex LNA circuitry and the poly-phase filter circuitry provides better image rejection, albeit with a somewhat higher loss. Thus, the choice of using the complex LNA circuitry and the poly-phase filter circuitry depends on a trade-off between image rejection and loss in the poly-phase filter circuitry.

The down-converter circuitry 409 mixes the amplified RF signal 827 with the RF local

oscillator signal 454, which it receives from the RF PLL circuitry 840. The down-converter circuitry 409 produces the in-phase analog down-converted signal 412 and the quadrature in-phase analog down-converted signal 415. The down-converter circuitry 409 provides the in-phase analog down-converted signal 412 and the quadrature in-phase analog down-converted signal 415 to a pair of programmable-gain amplifiers (PGAs) 833A and 833B.

The PGA 833A and PGA 833B in part allow for programming the gain of the receive

path. The PGA 833A and the PGA 833B supply an analog in-phase amplified signal 841 and an analog quadrature amplified signal 842 to complex ADC circuitry 836 (*i.e.*, both  $I$  and  $Q$  inputs will affect both  $I$  and  $Q$  outputs). The ADC circuitry 836 converts the analog in-phase amplified signal 841 into a one-bit in-phase digital receive signal 421. Likewise, the ADC circuitry 836 converts the analog quadrature amplifier signal 842 into a one-bit quadrature digital receive signal 424.

Note that RF transceivers and receivers according to the invention preferably use a one-bit digital interface. One may, however, use a variety of other interfaces, as persons skilled in the art who have the benefit of the description of the invention understand. For example, one may use a multi-bit interface or a parallel interface. Moreover, as described below, rather than, or in addition to, providing the one-bit in-phase and quadrature digital receive signals to the receiver digital circuitry 851, the digital interface between the receiver analog circuitry 839 and the receiver digital circuitry 851 may communicate various other signals. By way of illustration, those signals may include reference signals (e.g., clock signals), control signals, logic signals, hand-shaking signals, data signals, status signals, information signals, flag signals, and/or configuration signals. Furthermore, the signals may constitute single-ended or differential signals, as desired. Thus, the interface provides a flexible communication mechanism between the receiver analog circuitry and the receiver digital circuitry.

The receiver digital circuitry 851 accepts the one-bit in-phase digital receive signal 421

and the one-bit quadrature digital receive signal 424, and provides them to the digital down-converter circuitry 427. The digital down-converter circuitry 427 converts the received signals into a down-converted in-phase signal 430 and a down-converted quadrature signal 433 and provides those signals to the digital filter circuitry 436. The digital filter circuitry 436 preferably comprises an IIR channel-select filter that performs filtering operations on its input signals.

Note, however, that one may use other types of filters, for example, FIR filters, as desired.

The digital filter circuitry 436 provides the digital in-phase filtered signal 439 to a digital PGA 863A and the digital quadrature filtered signal 442 to a digital PGA 863B. The digital PGA 863A and PGA 863B in part allow for programming the gain of the receive path circuitry.

The digital PGA 863A supplies an amplified digital in-phase signal 869 to DAC circuitry 875A,

5 whereas the digital PGA 863B supplies an amplified digital quadrature signal 872 to DAC circuitry 875B. The DAC circuitry 875A converts the amplified digital in-phase signal 869 to the in-phase analog receive signal 448. The DAC circuitry 875B converts the amplified digital quadrature signal 872 signal into the quadrature analog receive signal 451. The baseband processor circuitry 120 accepts the in-phase analog receive signal 448 and the quadrature analog

10 receive signal 451 for further processing, as desired.

Note that the digital circuit blocks shown in the receiver digital circuitry 851 depict mainly the conceptual functions and signal flow. The actual digital-circuit implementation may or may not contain separately identifiable hardware for the various functional blocks. For

15 example, one may re-use (in time, for instance, by using multiplexing) the same digital circuitry to implement both digital PGA 863A and digital PGA 863B, as desired.

Note also that, similar to the RF transceiver in FIG. 4, the RF transceiver in FIG. 8

features a digital-IF architecture. The digital-IF architecture facilitates the implementation of the  
20 one-bit digital interface between the receiver digital circuitry 426 and the receiver analog circuitry 408. Moreover, the digital-IF architecture allows digital (rather than analog) IF-filtering, thus providing all of the advantages of digital filtering.

The transmitter circuitry 877 comprises baseband up-converter circuitry 466, transmit VCO circuitry 481, a pair of transmitter output buffers 892A and 892B, and offset PLL circuitry 897. The offset PLL circuitry 897 includes offset mixer circuitry 891, phase detector circuitry 882, and loop filter circuitry 886. The baseband up-converter circuitry 466 accepts the analog in-phase transmit input signal 460 and the analog quadrature transmit input signal 463, mixes those signals with the IF local oscillator signal 457, and provides a transmit IF signal 880 to the offset PLL circuitry 897. The offset PLL circuitry 897 uses the transmit IF signal 880 as a reference signal. The transmit IF signal 880 preferably comprises a modulated single-sideband IF signal but, as persons skilled in the art who have the benefit of the description of the invention understand, one may use other types of signal and modulation, as desired.

The offset mixer circuitry 891 in the offset PLL circuitry 897 mixes the transmit VCO output signal 478 with the RF local oscillator signal 454, and provides a mixed signal 890 to the phase detector circuitry 882. The phase detector circuitry 882 compares the mixed signal 890 to the transmit IF signal 880 and provides an offset PLL error signal 884 to the loop filter circuitry 886. The loop filter circuitry 886 in turn provides a filtered offset PLL signal 888 to the transmit VCO circuitry 481. Thus, the offset PLL circuitry 897 and the transmit VCO circuitry 481 operate in a feedback loop. Preferably, the output frequency of the transmit VCO circuitry 481 centers between the DCS and PCS bands, and its output is divided by two for the GSM band.

Transmitter output buffers 892A and 892B receive the transmit VCO output signal 478 and provide buffered transmit signals 894 and 895 to a pair of power amplifiers 896A and 896B. The power amplifiers 896A and 896B provide amplified RF signals 899 and 898, respectively, for transmission through antenna interface circuitry 202 and the antenna 130. Power amplifier 5 896A provides the RF signal 899 for the GSM band, whereas power amplifier 896B supplies the RF signal 898 for the DCS and PCS bands. Persons skilled in the art who have the benefit of the description of the invention, however, understand that one may use other arrangements of power amplifiers and frequency bands. Moreover, one may use RF filter circuitry within the output path of the transmitter circuitry 877, as desired.

10 The embodiment 800 comprises three circuit partitions, or circuit blocks. A first circuit partition 801 includes the receiver analog circuitry 839 and the transmitter circuitry 877. A second circuit partition 854 includes the receiver digital circuitry 851 and the reference generator circuitry 218. Finally, a third circuit partition comprises the local oscillator circuitry 222. The

15 first circuit partition 801, the second circuit partition 854, and the third circuit partition are partitioned from one another so that interference effects among the circuit partitions tend to be reduced. That arrangement tends to reduce the interference effects among the circuit partitions because of the analysis of interference effects provided above in connection with FIG. 3. Preferably, the first, second, and third circuit partitions each reside within an integrated circuit 20 device. To further reduce interference effects among the circuit partitions, the embodiment 800 in FIG. 8 uses differential signals wherever possible. The notation "(diff.)" adjacent to signal

lines or reference numerals in FIG. 8 denotes the use of differential lines to propagate the annotated signals.

Note that, similar to the RF transceiver shown in FIG. 4 and described above, the  
5 embodiment 800 shown in FIG. 8 uses an analog-digital-analog signal path in its receiver section. The embodiment 800 uses this particular signal path for reasons similar to those described above in connection with the transceiver shown in FIG. 4.

Like the transceiver in FIG. 4, if the receiver digital circuitry 851 need not be compatible

10 with the common analog interface to baseband processors, one may remove the DAC circuitry 875A and 875B, and use a digital interface to the baseband processor circuitry 120, as desired.

In fact, similar to the RF transceiver shown in FIG. 2D, one may realize the function of the receiver digital circuitry 851 within the baseband processor circuitry 120, using hardware,  
15 software, or a combination of hardware and software. In that case, the RF transceiver would include two circuit partitions, or circuit blocks. The first circuit partition 801 would include the receiver analog circuitry 839 and the transmitter circuitry 877. A second circuit partition would comprise the local oscillator circuitry 222. Note also that, similar to the RF transceiver shown in FIG. 2C, in the embodiment 800, one may include within the baseband processor circuitry 120 the functionality of the reference generator circuitry 218, as desired.

20

Another aspect of the invention includes a configurable interface between the receiver digital circuitry and the receiver analog circuitry. Generally, one would seek to minimize digital

switching activity within the receiver analog circuitry. Digital switching activity within the receiver analog circuitry would potentially interfere with the sensitive analog RF circuitry, for example, LNAs, or mixers. As described above, the receiver analog circuitry includes analog-to-digital circuitry (ADC), which preferably comprises sigma-delta-type ADCs. Sigma-delta ADCs typically use a clock signal at their output stages that generally has a pulse shape and, thus, contains high-frequency Fourier series harmonics. Moreover, the ADC circuitry itself produces digital outputs that the receiver digital circuitry uses. The digital switching present at the outputs of the ADC circuitry may also interfere with sensitive analog circuitry within the receiver analog circuitry.

The invention contemplates providing RF apparatus according to the invention, for example, receivers and transceivers, that include an interface circuitry to minimize or reduce the effects of interference from digital circuitry within the RF apparatus. FIG. 9A shows an embodiment 900A of an interface between the receiver digital circuitry 905 and the receiver

analog circuitry 910. The interface includes configurable interface signal lines 945. The baseband processor circuitry 120 in the transceiver of FIG. 9A communicates configuration, status, and setup information with both the receiver digital circuitry 905 and the receiver analog circuitry 910. In the preferred embodiments of RF transceivers according to the invention, the baseband processor circuitry 120 communicates with the receiver digital circuitry 905 and the receiver analog circuitry 910 by sending configuration data to read and write registers included within the receiver digital circuitry 905 and the receiver analog circuitry 910.

The receiver digital circuitry 905 communicates with the baseband processor circuitry 120 through a set of serial interface signal lines 920. The serial interface signal lines 920 preferably include a serial data-in (SDI) signal line 925, a serial clock (SCLK) signal line 930, a serial interface enable (SENB) signal line 935, and a serial data-out (SDO) signal line 940. The transceiver circuitry and the baseband processor circuitry 120 preferably hold all of the serial interface signal lines 920 at static levels during the transmit and receive modes of operation. The serial interface preferably uses a 22-bit serial control word that comprises 6 address bits and 16 data bits. Note, however, that one may use other serial interfaces, parallel interfaces, or other types of interfaces, that incorporate different numbers of signal lines, different types and sizes of signals, or both, as desired. Note also that, the SENB signal is preferably an active-low logic signal, although one may use a normal (*i.e.*, an active-high) logic signal by making circuit modifications, as persons skilled in the art understand.

The receiver digital circuitry 905 communicates with the receiver analog circuitry 910 via

configurable interface signal lines 945. Interface signal lines 945 preferably include four configurable signal lines 950, 955, 960, and 965, although one may use other numbers of configurable signal lines, as desired, depending on a particular application. In addition to supplying the serial interface signals 920, the baseband processor circuitry 120 provides a control signal 915, shown as a power-down (PDNB) signal in FIG. 9A, to both the receiver digital circuitry 905 and the receiver analog circuitry 910. The receiver digital circuitry 905 and the receiver analog circuitry 910 preferably use the power-down (PDNB) signal as the control signal 915 to configure the functionality of the interface signal lines 945. In other words, the

functionality of the interface signal lines 945 depends on the state of the control signal 915.

Also, the initialization of the circuitry within the receive path and the transmit path of the transceiver occurs upon the rising edge of the PDNB signal. Note that the PDNB signal is preferably an active-low logic signal, although one may use a normal (*i.e.*, an active-high) logic signal, as persons skilled in the art would understand. Note also that, rather than using the PDNB signal, one may use other signals to control the configuration of the interface signal lines 945, as desired.

In the power-down or serial interface mode (*i.e.*, the control signal 915 (for example,

10 PDNB) is in the logic low state), interface signal line 950 provides the serial clock (SCLK) and interface signal line 955 supplies the serial interface enable signal (SENB). Furthermore,

15 interface signal line 960 provides the serial data-in signal (SDI), whereas interface signal line 965 supplies the serial data-out (SDO) signal. One may devise other embodiments according to the invention in which, during this mode of operation, the transceiver may also perform circuit

calibration and adjustment procedures, as desired (for example, the values of various transceiver components may vary over time or among transceivers produced in different manufacturing batches. The transceiver may calibrate and adjust its circuitry to take those variations into account and provide higher performance).

20 In the normal receive mode of operation (*i.e.*, the control signal, PDNB, is in the logic-

high state), interface signal line 950 provides a negative clock signal (CKN) and interface signal line 955 supplies the positive clock signal (CKP). Furthermore, interface signal line 960

provides a negative data signal (ION), whereas interface signal line 965 supplies a positive data signal (IOP).

In preferred embodiments of the invention, the CKN and CKP signals together form a

- 5 differential clock signal that the receiver digital circuitry 905 provides to the receiver analog circuitry 910. The receiver analog circuitry 910 may provide the clock signal to the transmitter circuitry within the RF transceiver in order to facilitate calibration and adjustment of circuitry, as  
described above. During the receive mode, the receiver analog circuitry 910 provides the ION  
and IOP signals to the receiver digital circuitry 905. The ION and IOP signals preferably form a  
10 differential data signal. As noted above, the transceiver disables the transmitter circuitry during  
the receive mode of operation.

In preferred embodiments according to the invention, clock signals CKN and CKP are

- turned off when the transmitter circuitry is transmitting signals. During the transmit mode,  
15 interface signal lines 960 and 965 preferably provide two logic signals from the receiver digital circuitry 905 to the receiver analog circuitry 910. The signal lines may provide input/output signals to communicate data, status, information, flag, and configuration signals between the receiver digital circuitry 905 and the receiver analog circuitry 910, as desired. Preferably, the logic signals control the output buffer of the transmit VCO circuitry. Note that, rather than  
20 configuring interface signal lines 960 and 965 as logic signal lines, one may configure them in other ways, for example, analog signal lines, differential analog or digital signal lines, etc., as

desired. Furthermore, the interface signal lines 960 and 965 may provide signals from the receiver digital circuitry 905 to the receiver analog circuitry 910, or vice-versa, as desired.

In addition to using differential signals, RF transceivers according to the invention

5 preferably take other measures to reduce interference effects among the various transceiver circuits. Signals CKN, CKP, ION, and IOP may constitute voltage signals, as desired.

Depending on the application, the signals CKN, CKP, ION, and IOP (or logic signals in the transmit mode) may have low voltage swings (for example, voltage swings smaller than the supply voltage) to reduce the magnitude and effects of interference because of the voltage

10 switching on those signals.

In preferred embodiments according to the invention, signals CKN, CKP, ION, and IOP constitute current, rather than voltage, signals. Moreover, to help reduce the effects of interference even further, RF transceivers according to the invention preferably use band-limited

15 signals. RF transceivers according to the invention preferably use filtering to remove some of the higher frequency harmonics from those signals to produce band-limited current signals.

Table 3 below summarizes the preferred functionality of the configurable interface signal

lines 950, 955, 960, and 965 as a function of the state of the control signal 915 (for example,

20 PDNB):

<b>Signal Line</b>	<b>Control = 0</b>	<b>Control = 1 (During Reception)</b>	<b>Control = 1 (During Transmission)</b>
950	SCLK	CKN	(CKN off)
955	SENB	CKP	(CKP off)
960	SDI	ION	Logic Signal
965	SDO	IOP	Logic Signal

Table 3

Using configurable interface signal lines 945 in the interface between the receiver digital circuitry 905 and the receiver analog circuitry 910 allows using the same physical connections

5 (e.g., pins on an integrated-circuit device or electrical connectors on a module) to accomplish different functionality. Thus, the configurable interface between the receiver digital circuitry 905 and the receiver analog circuitry 910 makes available the physical electrical connections available for other uses, for example, providing ground pins or connectors around sensitive analog signal pins or connectors to help shield those signals from RF interference. Moreover, the

10 configurable interface between the receiver digital circuitry 905 and the receiver analog circuitry 910 reduces packaging size, cost, and complexity.

FIG. 9B shows an embodiment 900B that includes a configurable interface according to

the invention. Here, the baseband processor circuitry 120 subsumes the functionality of the  
15 receiver digital circuitry 905. The baseband processor circuitry 120 realizes the functionality of the receiver digital circuitry 905, using hardware, software, or both, as desired. Because the

baseband processor circuitry 120 has subsumed the receiver digital circuitry 905, the baseband processor circuitry 120 may communicate with the receiver analog circuitry 910 using configurable interface signal lines 945, depending on the state of the control signal 915 (*e.g.*, the PDNB signal). The configurable interface signal lines 945 perform the same functions described above in connection with FIG. 9A, depending on the state of the control signal 915. As noted above, one may reconfigure the interface signal lines 960 and 965 during transmit mode to implement desired functionality, for example, logic signals.

FIG. 10 shows a conceptual block diagram of an embodiment 1000 of a configurable

10 interface according to the invention within an RF transceiver in the power-down or serial  
15 interface mode (*i.e.*, the control signal 915 is in a logic-low state). A logic low state on the

control signal 915 enables the driver circuitry 1012A, 1012B, and 1012C, thus providing the  
configurable serial interface signal lines 950, 955, and 960 to the receiver analog circuitry 910.

20 Similarly, the logic low state on the control signal 915 causes the AND gates 1030A, 1030B, and  
15 1030C to provide configurable interface signal lines 950, 955, and 960 to other circuitry within

the receiver analog circuitry 910. The outputs of the AND gates 1030A, 1030B, and 1030C  
comprise a gated SCLK signal 1032, a gated SENB signal 1034, and a gated SDI signal 1036,  
respectively.

20 Interface controller circuitry 1040 accepts as inputs the gated SCLK signal 1032, the  
gated SENB signal 1034, and the gated SDI signal 1036. The interface controller circuitry 1040  
resides within the receiver analog circuitry 910 and produces a receiver analog circuitry SDO

signal 1044 and an enable signal 1046. By controlling tri-state driver circuitry 1042, the enable signal 1046 controls the provision of the receiver analog circuitry SDO signal 1044 to the receiver digital circuitry 905 via the configurable interface signal line 965.

5 Interface controller circuitry 1010 within the receiver digital circuitry 905 accepts the

SCLK signal 925, the SENB signal 930, and the SDI signal 935 from the baseband processor circuitry 120. By decoding those signals, the interface controller circuitry 1010 determines

whether the baseband processor circuitry 120 intends to communicate with the receiver digital

circuitry 905 (*e.g.*, the baseband processor circuitry 120 attempts to read a status or control

10 register present on the receiver digital circuitry 905). If so, the interface controller circuitry 1010

provides the SCLK signal 925, the SENB signal 930, and the SDI signal 935 to other circuitry

(not shown explicitly) within the receiver digital circuitry 905 for further processing.

Interface controller circuitry 1010 provides as output signals a receiver digital circuitry

15 SDO signal 1018, a select signal 1020, and an enable signal 1022. The receiver digital circuitry

SDO signal 1018 represents the serial data-out signal for the receiver digital circuitry 905, *i.e.*,

the serial data-out signal that the receiver digital circuitry 905 seeks to provide to the baseband

processor circuitry 120. The interface controller circuitry 1010 supplies the select signal 1020 to

multiplexer circuitry 1014. The multiplexer circuitry 1014 uses that signal to selectively provide

20 as the multiplexer circuitry output signal 1024 either the receiver digital circuitry SDO signal

1018 or the receiver analog circuitry SDO signal 1044, which it receives through configurable

interface signal line 965. Tri-state driver circuitry 1016 provides the multiplexer circuitry output signal 1024 to the baseband processor circuitry 120 under the control of the enable signal 1022.

Tri-state driver circuitry 1012A, 1012B, and 1012C use an inverted version of the control

5 signal 915 as their enable signals. Thus, a logic high value on the control signal 915 disables the driver circuitry 1012A, 1012B, and 1012C, thus disabling the serial interface between the

receiver digital circuitry 905 and the receiver analog circuitry 910. Similarly, AND gates 1030A,

10 1030B, and 1030C use an inverted version of the control signal 915 to gate interface signal lines

950, 955, and 960. In other words, a logic high value on the control signal 915 inhibits logic

15 switching at the outputs of AND gates 1030A, 1030B, and 1030C, which reside on the receiver analog circuitry 910.

FIG. 11A shows a conceptual block diagram of an embodiment 1100A of a configurable

20 interface according to the invention, in an RF transceiver operating in the normal receive mode

15 of operation (*i.e.*, the control signal 915 is in a logic-high state). As noted above, in this mode, the receiver digital circuitry 905 provides a clock signal to the receiver analog circuitry 910

through the configurable interface signal lines 950 and 955. Configurable interface signal line

950 provides the CKN signal, whereas configurable interface signal line 955 supplies the CKP

signal. Also in this mode, the receiver analog circuitry 910 provides a data signal to the receiver

20 digital circuitry 905 through the configurable interface signal lines 960 and 965.

The receiver digital circuitry 905 provides the CKN and CKP signals to the receiver analog circuitry 910 by using clock driver circuitry 1114. The clock driver circuitry 1114 receives a clock signal 1112A and a complement clock signal 1112B from signal processing circuitry 1110. Signal processing circuitry 1110 receives the reference signal 220 and converts it  
5 to the clock signal 1112A and complement clock signal 1112B. Interface controller circuitry 1116 provides an enable signal 1118 that controls the provision of the CKN and CKP clock signals to the receiver analog circuitry 910 via the interface signal lines 950 and 955, respectively.

10 Receiver analog circuitry 910 includes clock receiver circuitry 1130 that receives the CKN and CKP clock signals and provides a clock signal 1132A and a complement clock signal 1132B. Interface controller circuitry 1140 within the receiver analog circuitry 910 provides an enable signal 1142 that controls the operation of the clock receiver circuitry 1130.

15 The clock signal 1132A clocks the ADC circuitry 1144, or other circuitry (for example,

calibration circuitry), or both, as desired. Note that, rather than using the clock signal 1132A, one may use the complement clock signal 1132B, or both the clock signal 1132A and the complement clock signal 1132B, by making circuit modifications as persons skilled who have the benefit of the description of the invention understand. The ADC circuitry 1144 provides to

20 multiplexer circuitry 1150 a one-bit differential in-phase digital signal 1146A and a one-bit differential quadrature digital signal 1146B. The multiplexer circuitry 1150 provides a one-bit differential digital output signal 1152 to data driver circuitry 1154. The output signal 1152

therefore constitutes multiplexed *I*-channel data and *Q*-channel data. The data driver circuitry 1154 supplies the differential data signal comprising ION and IOP to the receiver digital circuitry 905, using the configurable interface signal lines 960 and 965, respectively.

5       The clock signal 1132A also acts as the select signal of multiplexer circuitry 1150. On alternating edges of the clock signal 1132A, the multiplexer circuitry 1150 selects, and provides to, the data driver circuitry 1154 the one-bit differential in-phase digital signal 1146A (*i.e.*, *I*-channel data) and the one-bit differential quadrature digital signal 1146B (*i.e.*, *Q*-channel data).

10      The interface controller circuitry 1140 supplies an enable signal 1156 to the data driver circuitry 1154 that controls the provision of the configurable interface signal 960 and the configurable interface signal 965 to the receiver digital circuitry 905 via the configurable interface signal lines 960 and 965.

15      The receiver digital circuitry 905 includes data receiver circuitry 1120. Data receiver

15      circuitry 1120 accepts from the receiver analog circuitry 910 the signals provided via the configurable interface signal lines 960 and 965. The data receiver circuitry 1120 provides a pair of outputs 1122A and 1122B. An enable signal 1124, supplied by the interface controller circuitry 1116, controls the operation of the data receiver circuitry 1120.

20      The receiver digital circuitry 905 also includes a delay-cell circuitry 1119 that accepts as its inputs the clock signal 1112A and the complement clock signal 1112B. The delay-cell circuitry 1119 constitutes a delay-compensation circuit. In other words, ideally, the signal-

propagation delay of the delay-cell circuitry 1119 compensates for the delays the signals experience as they propagate from the receiver digital circuitry 905 to the receiver analog circuitry 910, and back to the receiver digital circuitry 905.

5 The delay-cell circuitry 1119 provides as its outputs a clock signal 1121A and a

complement clock signal 1121B. The clock signal 1121A and the complement clock signal

1121B clock a pair of *D* flip-flop circuitries 1123A and 1123B, respectively. The *D* flip-flop

circuitries 1123A and 1123B latch the output 1122A of the data receiver circuitry 1120

alternately. In other words, the clock signal 1121A causes the latching of the *I*-channel data by

10 the *D* flip-flop circuitry 1123A, whereas the complement clock signal 1121B causes the *D* flip-

15 flop circuitry 1123B to latch the *Q*-channel data.

The output signals of the delay-cell circuitry 1119 help the receiver digital circuitry 905

20 to sample the *I*-channel data and the *Q*-channel data that it receives from the receiver analog

circuitry 910. The receiver digital circuitry 905 receives multiplexed *I*-channel data and the *Q*-

channel data through the ION signal 960 and the IOP signal 965. Thus, the *D* flip-flop circuitries

1123A and 1123B perform a de-multiplexing function on the multiplexed *I*-channel data and *Q*-

channel data.

25 In the normal receive or transmit modes, (*i.e.*, the control signal 915 is in the logic-high

state), interface signal line 950 provides the negative clock signal (CKN) and interface signal line

855 supplies the positive clock signal (CKP). In preferred embodiments of the invention, the

CKN and CKP signals together form a differential clock signal that the receiver digital circuitry 905 provides to the receiver analog circuitry 910.

During the receive mode, interface signal line 960 provides the negative data signal 5 (ION), whereas interface signal line 965 supplies the positive data signal (IOP). The ION and IOP signals preferably form a differential data signal.

In the transmit mode, the data signal may function as an input/output signal to communicate data, status, information, flag, and/or configuration signals between the receiver 10 digital circuitry 905 and the receiver analog circuitry 910. Preferably, the interface signal lines 960 and 965 function as two logic signal lines in the transmit mode. As noted above, the transceiver disables the receiver circuitry during the transmit mode of operation. In RF 15 transceivers partitioned according to the invention (see, e.g., FIGS. 2A-2D, 4, and 8), the clock receiver circuitry 1130 may provide the clock signal 1132A, the complement clock signal 1132B, or both, to transmitter circuitry (partitioned together with the receiver analog circuitry 910) for 20 circuit calibration, circuit adjustment, and the like, as described above.

In the transmit mode, once circuit calibration and adjustment has concluded, however, the clock driver circuitry 1114 uses the enable signal 1118 to inhibit the propagation of the CKN and 25 CKP clock signals to the receiver analog circuitry 910. In this manner, the clock driver circuitry 1114 performs the function of the switch 492 in FIGS. 4 and 8. Note that, during the normal transmit mode of operation, the ADC circuitry 1144 does not provide any data to the receiver

digital circuitry 905 via the ION and IOP signals because, according to the TDD protocol, the receiver path circuitry is inactive during the normal transmit mode of operation. Instead, the receiver digital circuitry 905 provides control signals to the receiver analog circuitry 910 via interface signal lines 960 and 965.

5

During the transmit mode, the interface controller circuitry 1116 provides control signals

via signal lines 1160 to the interface signal lines 960 and 965. The interface controller circuitry

1140 receives the control signals via signal lines 1165 and provides them to various blocks

within the receiver analog circuitry, as desired. During the receive mode, the interface controller

10 circuitry 1116 inhibits (e.g., high-impedance state) the signal lines 1160. Similarly, the interface

controller circuitry 1140 inhibits the signal lines 1165 during the receive mode.

For the purpose of conceptual illustration, FIG. 11A shows the interface controller

15 circuitry 1116 and the interface controller circuitry 1140 as two blocks of circuitry distinct from

the interface controller circuitry 1010 and the interface controller circuitry 1040 in FIG. 10,

respectively. One may combine the functionality of the interface controller circuitry 1116 with

the functionality of the interface controller circuitry 1010, as desired. Likewise, one may

combine the functionality of interface controller circuitry 1140 with the functionality of the

interface controller circuitry 1040, as desired. Moreover, one may combine the functionality of

20 the signal processing circuitries 1110 with the functionality of the interface controller circuitry

1116 and the interface controller circuitry 1140, respectively. Combining the functionality of

those circuits depends on various design and implementation choices, as persons skilled in the art understand.

FIG. 11B illustrates a block diagram of a preferred embodiment 1100B of a delay-cell

5 circuitry 1119 according to the invention. The delay-cell circuitry 1119 includes a replica of the

clock driver circuitry 1114A in tandem with a replica of the data receiver circuitry 1120A. In

other words, the block labeled "1114A" is a replica of the clock driver circuitry 1114, and the

block labeled "1120A" is a replica of the data receiver circuitry 1120. (Note that the delay-cell

circuitry 1119 may alternatively include a replica of the data driver circuitry 1154 in tandem with

10 a replica of the clock receiver circuitry 1130.) The replica of the clock driver circuitry 1114A

accepts the clock signal 1112A and the complement clock signal 1112B. The replica of the clock

driver circuitry 1114A provides its outputs to the replica of the data receiver circuitry 1120A.

The replica of the data receiver circuitry 1120A supplies the clock signal 1121A and the

complement clock signal 1121B. The clock signal 1121A and the complement clock signal

15 1121B constitute the output signals of the delay-cell circuitry 1119. The delay-cell circuitry

1119 also receives as inputs enable signals 1118 and 1124 (note that FIG. 11A does not show

those input signals for the sake of clarity). The enable signal 1118 couples to the replica of the

clock driver circuitry 1114A, whereas the enable signal 1124 couples to the replica of the data

receiver circuitry 1120A.

20

Note that FIG. 11B constitutes a conceptual block diagram of the delay-cell circuitry

1119. Rather than using distinct blocks 1114A and 1120A, one may alternatively use a single

block that combines the functionality of those two blocks, as desired. Moreover, one may use a circuit that provides an adjustable, rather than fixed, delay, as desired. Note also that the embodiment 1100B of the delay-cell circuitry 1119 preferably compensates for the delay in the clock driver circuitry 1114 in FIG. 11A. In other words, the delay-cell circuitry 1119 preferably

5 compensates sufficiently for the round-trip delay in the signals that travel from the receiver digital circuitry 905 to the receiver analog circuitry 910 and back to the receiver digital circuitry 905 to allow for accurate sampling in the receiver digital circuitry of the *I*-channel data and the *Q*-channel data. Note that in the embodiment 1100B, the replica of the clock driver circuitry 1114A mainly compensates for the round-trip delay, whereas the replica of the data receiver

10 circuitry 1120A converts low-swing signals at the output of the replica of the clock driver circuitry 1114A into full-swing signals.

The receiver digital circuitry 905 and the receiver analog circuitry 910 preferably reside

15 within separate integrated-circuit devices. Because those integrated-circuit devices typically result from separate semiconductor fabrication processes and manufacturing lines, their process parameters may not match closely. As a result, the preferred embodiment 1100B of the delay-cell circuitry 1119 does not compensate for the delay in the clock receiver circuitry 1130, the data driver circuitry 1154, and the data receiver circuitry 1120 in FIG. 11A.

20 Note, however, that if desired, the delay-cell circuitry 1119 may also compensate for the signal delays of the clock receiver circuitry 1130, the data driver circuitry 1154, and the data receiver circuitry 1120. Thus, in situations where one may match the process parameters of the

receiver digital circuitry 905 and the receiver analog circuitry 910 relatively closely (for example, by using thick-film modules, silicon-on-insulator, etc.), the delay-cell circuitry 1119 may also compensate for the delays of other circuit blocks. As another alternative, one may use a delay-cell circuitry 1119 that provides an adjustable delay and then program the delay based on

5 the delays in the receiver digital circuitry 905 and the receiver analog circuitry 910 (e.g., provide a matched set of receiver digital circuitry 905 and receiver analog circuitry 910), as persons skilled in the art who have the benefit of the description of the invention understand.

Furthermore, rather than an open-loop arrangement, one may use a closed-loop feedback circuit implementation (e.g., by using a phase-locked loop circuitry) to control and compensate for the

10 delay between the receiver analog circuitry 910 and the receiver digital circuitry 905, as desired.

Note that the digital circuit blocks shown in FIGS. 11A and 11B depict mainly the conceptual functions and signal flow. The actual circuit implementation may or may not contain separately identifiable hardware for the various functional blocks. For example, one may

15 combine the functionality of various circuit blocks into one circuit block, as desired.

FIG. 12 shows a schematic diagram of a preferred embodiment 1200 of a signal-driver circuitry according to the invention. One may use the signal-driver circuitry as the clock driver circuitry 1114 and the data driver circuitry 1154 in FIG. 11A. In the latter case, the input signals to the signal-driver circuitry constitute the output signals 1152 and the enable signal 1156, whereas the output signals of the signal-receiver circuitry constitute the ION and IOP signals 960 and 965, respectively, in FIG. 11A.

The signal-driver circuitry in FIG. 12 constitutes two circuit legs. One circuit leg includes MOSFET devices 1218 and 1227 and resistor 1230. The second leg includes MOSFET devices 1242 and 1248 and resistor 1251. The input clock signal controls MOSFET devices 5 1218 and 1242. Current source 1206, MOSFET devices 1209 and 1215, and resistor 1212 provide biasing for the two circuit legs.

MOSFET devices 1227 and 1248 drive the CKN and CKP output terminals through

resistors 1230 and 1251, respectively. Depending on the state of the clock signal, one leg of the  
10 signal-driver circuitry conducts more current than the other leg. Put another way, the signal-  
driver circuitry steers current from one leg to the other in response to the clock signal (*i.e.*, in  
response to the clock signal, one leg of the circuit turns on and the other leg turns off, and vice-  
versa). As a result, the signal-driver circuitry provides a differential clock signal that includes  
15 current signals CKN and CKP.

If the enable signal is high, MOSFET device 1203 is off and therefore does not affect the

operation of the rest of the circuit. In that case, a current  $I_O$  flows through the current source  
20 1206 and diode-connected MOSFET device 1209. The flow of current generates a voltage at the  
gate of MOSFET device 1209. MOSFET devices 1227 and 1248 share the same gate connection  
with MOSFET device 1209. Thus, MOSFET devices 1227 and 1248 have the same gate-source  
voltage,  $V_{gs}$ , as MOSFET device 1209 when the appropriate MOSFET devices are in the on  
state.

MOSFET devices 1218 and 1242 cause current steering between the first and second circuit legs. Only one of the MOSFET devices 1218 and 1242 is in the on state during the operation of the circuit. Depending on which MOSFET device is in the on state, the mirroring 5 current  $I_O$  flows through the circuit leg that includes the device in the on state.

Resistors 1221 and 1239 provide a small trickle current to the circuit leg that includes the MOSFET device (*i.e.*, MOSFET device 1218 or MOSFET device 1242) that is in the off state.

The small trickle current prevents the diode-connected MOSFET devices in the signal receiver 10 circuitry (see FIG. 13) from turning off completely. The trickle current helps to reduce the delay in changing the state of the circuit in response to transitions in the input clock signal. The trickle currents also help to reduce transient signals at the CKP and CKN terminals and, thus, reduce interference effects.

15 Capacitors 1224 and 1245 provide filtering so that when MOSFET device 1218 and MOSFET device 1242 switch states, the currents through the first and second circuit legs (CKN and CKP circuit legs) do not change rapidly. Thus, capacitors 1224 and 1245 reduce the high-frequency content in the currents flowing through the circuit legs into the CKN and CKP terminals. The reduced high-frequency (*i.e.*, band-limited) content of the currents flowing 20 through the CKN and CKP terminals helps reduce interference effects to other parts of the circuit, for example, the LNA circuitries, as described above. Capacitors 1233 and 1236 and resistors 1230 and 1251 help to further reduce the high-frequency content of the currents flowing

through the CKN and CKP terminals. Thus, the circuit in FIG. 12 provides smooth steering of current between the two circuit legs and therefore reduces interference effects with other circuitry.

5 When the enable signal goes to the low state, MOSFET device 1203 turns on and causes MOSFET device 1209 to turn off. MOSFET devices 1227 and 1248 also turn off, and the circuit becomes disabled. Note that the enable signal may be derived from the power-down PDNB signal.

10 FIG. 13A shows a schematic diagram of an exemplary embodiment 1300A of a signal-receiver circuitry according to the invention. One may use the signal-receiver circuitry as the clock receiver circuitry 1130 and the data receiver circuitry 1120 in FIG. 11A. In the latter case, the input signals to the signal-receiver circuitry constitute the ION and IOP signals 960 and 965 and the enable signal 1124, whereas the output signals constitute the signals at the outputs 1122A and 1122B, respectively, in FIG. 11A.

15 The signal receiver circuitry in FIG. 13A helps to convert differential input currents into CMOS logic signals. The signal-receiver circuitry in FIG. 13A constitutes two circuit legs. The first circuit leg includes MOSFET devices 1303, 1342, and 1345. The second leg includes 20 MOSFET devices 1309, 1324, and 1327. Note that, preferably, the scaling of MOSFET devices 1303 and 1309 provides a current gain of 1:2 between them. Likewise, the scaling of MOSFET

devices 1330 and 1327 preferably provides a current gain of 1:2 between them. The current gains help to reduce phase noise in the signal-receiver circuitry.

MOSFET devices 1339, 1342, 1333, and 1324 provide enable capability for the circuit.

- 5 When the enable input is in the high state, MOSFET devices 1339, 1342, 1333, and 1324 are in the on state. MOSFET devices 1345 and 1336 are current mirrors, as are MOSFET devices 1303 and 1309. MOSFET devices 1330 and 1327 also constitute current mirrors.

The currents flowing through the CKN and CKP terminals mirror to the MOSFET

- 10 devices 1327 and 1309. The actual current flowing through the second circuit leg depends on the currents that MOSFET device 1327 and MOSFET device 1309 try to conduct; the lower of the two currents determines the actual current that flows through the second circuit leg.

The difference between the currents that MOSFET device 1327 and MOSFET device

- 15 1309 try to conduct flows through the parasitic capacitance at node 1360. The current flow charges or discharges the capacitance at node 1360, thus making smaller the drain-source voltage ( $V_{ds}$ ) of whichever of MOSFET devices 1327 and 1309 that seeks to carry the higher current. Ultimately, the lower of the currents that MOSFET devices 1327 and 1309 seek to conduct determines the current through the second leg of the circuit.

A pair of inverters 1312 and 1315 provide true and complement output signals 1351 and 1348, respectively. The signal receiver circuitry therefore converts differential input currents into CMOS logic output signals.

5 In exemplary embodiments of the invention, the signal receiver circuitry provides fully

differential output signals. FIG. 13B shows an embodiment 1300B of such a signal receiver circuitry. One may use embodiment 1300B in a similar manner and application as embodiment

10 1300A, using the same input signals, as desired. Unlike embodiment 1300A, however,

embodiment 1300B includes fully differential circuitry to generate fully differential output

signals.

Embodiment 1300B includes the same devices as does embodiment 1300A, and the common devices operate in a similar manner. Furthermore, embodiment 1300B includes additional devices and components. Embodiment 1300B constitutes two circuit legs and replica

15 of those circuit legs. The first circuit leg includes MOSFET devices 1303, 1342, and 1345. The

replica of the first circuit leg includes devices 1355, 1379, and 1381. The second circuit leg

includes MOSFET devices 1309, 1324, and 1327. The replica of the second circuit leg include

devices 1357, 1363, and 1365. The scaling of MOSFET devices 1303 and 1309 provides a

current gain of 1:2 between them, as does the scaling of MOSFET devices 1330 and 1327.

20 Likewise, scaling of MOSFET devices 1355 and 1357 provides a current gain of 1:2 between

them, as does the scaling of MOSFET devices 1336 and 1365. The current gains help to reduce

phase noise in the signal-receiver circuitry.

Embodiment 1300B generally operates similarly to embodiment 1300A. Devices 1381, 1379, 1355, 1353, 1357, 1363, 1365, 1367, 1369, 1359, and 1361 perform the same functions as do devices 1345, 1342, 1303, 1306, 1309, 1324, 1327, 1321, 1318, 1312, and 1315, respectively.

- 5 The enable function also operates similarly to embodiment 1300A. Resistors 1371 and 1375 and capacitors 1373 and 1377 filter the input clock (*e.g.*, 13 MHz clock). Inverters 1312, 1315, 1361, and 1359 provide fully differential true and complement output signals.

FIG. 14 shows an embodiment 1400 of an alternative signal-driver circuitry according to

10 the invention. The signal-driver circuitry in FIG. 14 includes two circuit legs. The first circuit leg includes MOSFET device 1406 and resistor 1415A. The second circuit leg includes MOSFET device 1409 and resistor 1415B. A current source 1403 supplies current to the two circuit legs.

15 The input clock signal controls MOSFET devices 1406 and 1409. MOSFET devices

1406 and 1409 drive the CKP and CKN output terminals, respectively. Depending on the state of the clock signal, one leg of the signal-driver circuitry conducts current. Put another way, the signal-driver circuitry steers current from one leg to the other in response to the clock signal. As a result, the signal-driver circuitry provides a differential clock signal that includes signals CKN

20 and CKP. Capacitor 1412 filters the output signals CKN and CKP. Put another way, capacitor 1412 provides band-limiting of the output signals CKN and CKP. Note that the current source

1403 supplies limited-amplitude signals by providing current through resistors 1415A and 1415B.

Note that the signal-driver circuitries (clock driver and data driver circuitries) according

5 to the invention preferably provide current signals CKN and CKP. Similarly, signal-receiver circuitries (clock receiver and data receiver circuitries) according to the invention preferably receive current signals. As an alternative, one may use signal-driver circuitries that provide as their outputs voltage signals, as desired. One may also implement signal-receiver circuitries that receive voltage signals, rather than current signals. As noted above, depending on the  
10 application, one may limit the frequency contents of those voltage signals, for example, by filtering, as desired.

Generally, several techniques exist for limiting noise, for example, digital switching-

noise, in the interface between the receiver analog circuitry and the receiver digital circuitry

15 according to the invention. Those techniques include using differential signals, using band-limited signals, and using amplitude-limited signals. RF apparatus according to the invention may use any or all of those techniques, as desired. Furthermore, one may apply any or all of those techniques to interface circuitry that employs voltage or current signals, as persons of ordinary skill in the art who have the benefit of the description of the invention understand.

20 Note also that the RF transceiver embodiments according to the invention lend

themselves to various choices of circuit implementation, as a person skilled in the art who have

the benefit of the description of the invention understand. For example, as noted above, each of the circuit partitions, or circuit blocks, of RF transceivers partitioned according to the invention, resides preferably within an integrated circuit device. Persons skilled in the art, however, will appreciate that the circuit partitions, or circuit blocks, may alternatively reside within other substrates, carriers, or packaging arrangements. By way of illustration, other partitioning arrangements may use modules, thin-film modules, thick-film modules, isolated partitions on a single substrate, circuit-board partitions, and the like, as desired, consistent with the embodiments of the invention described here.

One aspect of the invention contemplates partitioning RF transceivers designed to operate within several communication channels (*e.g.*, GSM, PCS, and DCS). Persons skilled in the art, however, will recognize that one may partition according to the invention RF transceivers designed to operate within one or more other channels, frequencies, or frequency bands, as desired.

Moreover, the partitioning of RF transceivers according to the invention preferably applies to RF apparatus (*e.g.*, receivers or transceivers) with a low-IF, digital-IF architecture.

Note, however, that one may apply the partitioning and interfacing concepts according to the invention to other RF receiver or transceiver architectures and configurations, as persons of ordinary skill in the art who have the benefit of the description of the invention understand. By way of illustration, one may use the partitioning and interface concepts according to the invention in RF apparatus that includes:

- low-IF receiver circuitry;
- low-IF receiver circuitry and offset-PLL transmitter circuitry;
- low-IF receiver circuitry and direct up-conversion transmitter circuitry;
- direct-conversion receiver circuitry;
- direct-conversion receiver circuitry and offset-PLL transmitter circuitry; or
- direct-conversion receiver circuitry and direct up-conversion transmitter circuitry.

As an example of the flexibility of the partitioning concepts according to the invention,

one may include the LO circuitry in one partition, the receiver digital circuitry in a second

partition, and the transmitter up-converter circuitry and the receiver analog circuitry in a third

partition. As another illustrative alternative, one may include the LO circuitry and the transmitter

up-converter circuitry within one circuit partition, depending on the noise and interference

characteristics and specifications for a particular implementation.

Note that, in a typical direct-conversion RF receiver or transceiver implementation, the

receiver digital circuitry would not include the digital down-converter circuitry (the receiver

analog circuitry, however, would be similar to the embodiments described above). Furthermore,

in a typical direct up-conversion transmitter circuitry, one would remove the offset PLL circuitry

and the transmit VCO circuitry from the transmitter circuitry. The LO circuitry would supply the

RF LO signal to the up-conversion circuitry of the transmitter circuitry, rather than the offset-

PLL circuitry. Also, in a direct up-conversion implementation, the LO circuitry typically does

not provide an IF LO signal.

Furthermore, as noted above, one may use the partitioning and interface concepts according to the invention not only in RF transceivers, but also in RF receivers for high-performance applications. In such RF receivers, one may partition the receiver as shown in FIGS. 2A-2D and 4-8, and as described above. In other words, the RF receiver may have a first circuit partition that includes the receiver analog circuitry, and a second circuit partition that includes the receiver digital circuitry.

The RF receiver may also use the digital interface between the receiver analog circuitry

and the receiver digital circuitry, as desired. By virtue of using the receiver analog circuitry and the receiver digital circuitry described above, the RF receiver features a low-IF, digital-IF architecture. In addition, as noted above with respect to RF transceivers according to the invention, depending on performance specifications and design goals, one may include all or part of the local oscillator circuitry within the circuit partition that includes the receiver analog circuitry, as desired. Partitioning RF receivers according to the invention tends to reduce the interference effects between the circuit partitions.

As noted above, although RF apparatus according to the invention use a serial interface

between the receiver analog circuitry and the receiver digital circuitry, one may use other types of interface, for example, parallel interfaces, that incorporate different numbers of signal lines, different types and sizes of signals, or both, as desired. Moreover, the clock driver circuitries and the data driver circuitries may generally constitute signal-driver circuitries that one may use in a

RECEIVER APPARATUS AND CIRCUITRY

variety of digital interfaces between the receiver analog circuitry and the receiver digital circuitry according to the invention.

Likewise, the clock receiver circuitries and data receiver circuitries may generally

5 constitute signal-receiver circuitries that one may use in a variety of digital interfaces between the receiver analog circuitry and the receiver digital circuitry according to the invention. In other words, one may use signal-driver circuitries and signal-receiver circuitries to implement a wide variety of digital interfaces, as persons of ordinary skill who have the benefit of the description of the invention understand.

10 Another aspect of the invention relates to the circuitry within the local oscillator circuitry

15 222. Typically, in prior art LO circuitries, the attributes of the LO circuitry, such as the output power, exhibit variations over physical or environmental changes, such as semiconductor process variations or temperature. Variations in the output power of the LO circuitry, however, degrade performance of the RF apparatus.

For example, if one were to use conventional LO circuitries as LO circuitry 222 (see

FIGS. 2, 4-8), the output power of the RF local oscillator signal 224 and the IF local oscillator signal 226 (*i.e.*, the output power of the local oscillator circuitry 222) would exhibit variations over process and temperature. To avoid the resulting degradation of performance, the inventive concepts described here provide output buffer circuitries that exhibit a relatively constant output power over variations in physical and environmental conditions. Consequently, by reducing the

variations of the output power of the LO circuitry 222 over physical and environmental changes, the present invention provides an improved overall performance.

FIG. 15 shows a portion of a prior-art local-oscillator circuitry that includes output buffer

5      circuitry 1500. The output buffer circuitry 1500 includes VCO circuitry 1505, buffer circuitry 1510, voltage regulator circuitry 1520, PMOS transistor 1525, and NMOS transistor 1530. The output buffer circuitry 1500 drives a load 1535 ( $Z_L$ ). The buffer circuitry 1510 buffers the output signal of VCO circuitry 1505 and provides the resulting signal to the PMOS transistor 1525 and NMOS transistor 1530. The voltage regulator circuitry 1520 supplies a regulated voltage to the  
10     PMOS transistor 1525 and NMOS transistor 1530. In response to the variations in the output signal of the buffer circuitry 1510, the output buffer circuitry 1500 supplies an output signal to the load 1535.

Variations in the output power of the output buffer circuitry 1500 typically occur for two

15    reasons. First, the output signal of the VCO circuitry 1505 may vary with process and temperature and thus cause changes in the output power of the output buffer circuitry 1500.

Second, various components in the voltage regulator circuitry 1520 may cause changes in the current that the output buffer circuitry 1500 delivers to load 1535. For example, the output voltage of the voltage regulator circuitry 1520 may vary over process and temperature, thus

20    changing the voltage delivered to PMOS transistor 1525 and NMOS transistor 1530.

Furthermore, the electrical characteristics of the PMOS transistor 1525 and NMOS transistor

1530 may vary over process and temperature. As a consequence, the output power of the output buffer circuitry 1500 will vary.

FIG. 16 shows an embodiment 1600 of the output circuitry of an LO circuitry according

5 to invention that helps to reduce variations in the output power of the LO circuitry. The embodiment 1600 includes VCO circuitry 1505, output buffer circuitry 1605, voltage regulator circuitry 1610, voltage regulator circuitry 1615, and power measurement circuitry 1620. The VCO circuitry 1505 drives an input of the output buffer circuitry 1605. The output buffer circuitry 1605 supplies an output signal 1625 to load 1535. The output buffer circuitry includes a  
10 pair of complementary switches, for example, an NMOS transistor and a PMOS transistor (not shown explicitly).

Voltage regulator circuitry 1610 provides a regulated voltage 1610A to the VCO circuitry

1505. Similarly, voltage regulator circuitry 1615 provides a regulated voltage 1615A to the

15 output buffer circuitry 1605. Power measurement circuitry 1620 monitors the output power of output signal 1625 and provides control signal 1620A. Power measurement circuitry 1620, voltage regulator circuitry 1610, and voltage regulator circuitry 1615 form a feedback loop.

Voltage regulator circuitry 1610 uses the control signal 1620A to adjust its output voltage

1610A. Likewise, voltage regulator circuitry 1615 uses the control signal 1620A to adjust output

20 voltage 1615A. Note that control signal 1620A may include more than one signal, for example, it may include one signal for controlling voltage regulator circuitry 1610 and another signal for controlling voltage regulator circuitry 1615, as desired.

Variations in the output signal 1625 result in changes in the control signal 1620A, which consequently causes changes in the output voltage 1610A and output voltage 1615A that tend to offset or cancel the effect of the variation in the output signal 1625. The negative feedback loop 5 that contains power measurement circuitry 1620, voltage regulator circuitry 1610, and voltage regulator circuitry 1615 provides a way of reducing variations in the output power of the output signal 1625. Thus, the output buffer circuitry 1605 in the embodiment 1600 supplies a relatively constant power to the load 1535.

Note that the embodiment 1600 uses a circuit for measuring power (*i.e.*, power measurement circuitry 1620) of an RF signal. Designing and implementing a circuit for measuring RF power poses a relatively challenging task. Furthermore, the feedback loop in the embodiment 1600 operates continuously to keep the power level of the output signal 1625 relatively constant. The continuous operation of the feedback loop, however, may in some 15 situations contribute to reduced spectral purity of the output signal of VCO circuitry 1505.

FIG. 17 illustrates an embodiment 1700 of an output buffer circuitry according to the invention. Unlike embodiment 1600 (see FIG. 16), embodiment 1700 has a simpler architecture and does not use a power-measurement device. Embodiment 1700 includes a capacitor 1705, a 20 current source 1710, switch 1715 ( $S_1$ ), and switch 1720 ( $S_2$ ). Current source 1710 supplies a current  $I$  from a supply voltage,  $V_{DD}$ . Current source 1710 provides a relatively constant current

*I* over physical and environmental variations (e.g., process and temperature variations), using circuitry and techniques known to persons of ordinary skill in the art.

Output buffer circuitry 1700 drives load 1535. Switch 1715 and switch 1720 are  
5 controllable switches and respond to a control signal. An output signal 1505A of VCO circuitry  
1505 serves as the control signal for switch 1715 and switch 1720. One terminal of switch 1715  
couples to a reference terminal 1730 (e.g., ground or  $V_{SS}$ ). Another terminal of switch 1720  
couples to one terminal of switch 1720, and the resulting node supplies output signal 1725 of  
output buffer circuitry 1700. Another terminal of switch 1720 couples to one terminal of current  
10 source 1710 and to one terminal of capacitor 1705. A second terminal of capacitor 1705 couples  
to the reference terminal 1730.

Switch 1715 and switch 1720 operate in a complementary fashion. Assuming a mainly  
capacitive load, when switch 1715 is off and switch 1720 is on, current source 1710 delivers  
15 current  $I$  to the load 1535. Conversely, when switch 1715 is on, and switch 1720 is off, the load  
1535 discharges through switch 1715. In exemplary embodiments of the invention, switch 1715  
and switch 1720 each operate with a duty cycle of 50% (i.e., half of the cycle each).

Capacitor 1705 has a relatively large capacitance in order to reduce the ripple at node  
20 1750. In a practical implementation, capacitor 1705 acts as a high impedance at relatively low  
frequencies, i.e., at frequencies well below the frequency of the output signal of VCO circuitry  
1505. At relative low frequencies, current source 1710 provides current  $I$ . Thus, as relatively

low frequencies, capacitor 1705 allows the voltage at node 1750 to compensate for physical or environmental changes by making the current through switch 1720 constant on average. At relatively high frequencies, *i.e.*, at the frequency of the output signal of VCO circuitry 1505, capacitor 1705 constitutes a low-impedance source, and thus acts like a source of voltage.

5

At relatively low frequencies, *i.e.*, at frequencies well below the frequency of the output

signal of VCO circuitry 1505, current source 1710 acts as a current source. At relatively high

frequencies, *i.e.*, at the frequency of the output signal of VCO circuitry 1505, capacitor 1705

provides a relatively low impedance to ground and bypasses current source 1710. One may

10 consider the combination of current source 1710 and capacitor 1705 as a single source that acts

like a source of current (with high output impedance) at relatively low frequencies (frequencies

well below the frequency of the output signal of VCO circuitry 1505), and like a source of

voltage (with low output impedance) at relatively high frequencies (at the frequency of the output

15 signal of VCO circuitry 1505).

15

Assuming that the circuit has been operating at steady state, and assuming a 50% duty

cycle for switches 1715 and 1720, when switch 1720 closes, switch 1715 opens. Capacitor 1705

and current source 1710 each provide a current  $I$  to switch 1720, which provides the resulting

current  $2I$  to the load 1535. When switch 1720 opens and switch 1715 closes, the load 1535

20 discharges current  $2I$  through switch 1715. Because capacitor 1705 does not conduct any DC

current, switch 1720 on average delivers current  $I$  to the load 1535. Likewise, on average switch

1715 discharges current  $I$  from the load. Because of the indirect feedback action (described

below in detail in connection with FIG. 18), embodiment 1700 delivers to the load 1535 an output signal with a relatively constant power level.

FIG. 18 shows another embodiment 1800 of an output buffer circuitry 1800 according to

5 the invention. Embodiment 1800 generally operates in a manner similar to embodiment 1700 in  
FIG. 17, but includes further refinements. Embodiment 1800 includes capacitor 1810 ( $C_1$ ), a  
complementary transistor pair that includes NMOS transistor 1815 and PMOS transistor 1820,  
resistor 1825, current source 1710, and capacitor 1705 ( $C_2$ ). The output buffer circuitry in  
embodiment 1800 receives its input signal from a buffer 1805, and drives a load 1535 at its  
10 output.

Buffer 1805 receives an output signal of VCO circuitry 1505, buffers the output signal,

and provides the output signal to one terminal of capacitor 1810 ( $C_1$ ). The other terminal of

capacitor 1810 couples to the gate terminals of NMOS transistor 1815 and PMOS transistor 1820

15 and to one terminal of resistor 1825. The drain terminals of NMOS transistor 1815 and PMOS  
transistor 1820 drive load 1535. Current source 1710 provides current  $I$  to the source terminal of  
PMOS transistor 1820 and to one terminal of capacitor 1705. The second terminal of capacitor  
1705 couples to the reference terminal 1730. The source terminal of NMOS transistor 1815 also  
couples to the reference terminal 1730.

20

Capacitor 1810 ( $C_1$ ) couples the output of buffer 1805 to the gate terminals of NMOS  
transistor 1815 and PMOS transistor 1820. Because of the AC-coupling provided by capacitor

1810, the voltage swings at node 1830 and node 1835 can have different average values and amplitudes. Current source 1710 and Capacitor 1705 ( $C_2$ ) perform similar functions to the functions described above. Resistor 1825 biases NMOS transistor 1815 and PMOS transistor 1820 (in the absence of resistor 1825, node 1830 may have an undefined or floating voltage).

5

FIGS. 19A-B show equivalent circuits for the situation when one or the other of the two MOS transistors conducts. As noted above, NMOS transistor 1815 and PMOS transistor 1820 operate in a complementary manner. In other words, when NMOS transistor 1815 conducts, PMOS transistor 1820 is in the off state, and vice-versa. FIG. 19A pertains to when NMOS 10 transistor 1815 is off and PMOS transistor 1820 is in the on state. Because PMOS transistor 1820 is on, it couples node 1835 to node 1840, resulting in the circuit arrangement shown in FIG. 19A. Assuming that the circuit has been operating in steady-state condition when PMOS transistor 1820 turns on, capacitor 1705 delivers a current  $I$  to node 1835. Current source 1710 also delivers a current  $I$  to node 1835. As a result, a current  $2I$  flows through the load 1535. The 15 voltage at node 1535 rises nearly linearly (assuming a capacitive load 1535).

FIG. 19B illustrates an equivalent circuit when NMOS transistor 1815 is on and PMOS transistor 1820 is in the off state. Because NMOS transistor 1820 is on, it couples node 1835 to reference terminal 1730. Consequently, the load 1535 discharges into the reference terminal 20 1730. Furthermore, because PMOS transistor 1820 is off, current source 1710 delivers the current  $I$  to capacitor 1705 and charges capacitor 1705. As a result, the voltage at node 1840 rises nearly linearly.

FIG. 19C shows waveforms corresponding to various signals in FIGS. 19A-19B.

Waveform 1920 corresponds to the signal at node 1845 in the circuit shown in FIG. 18.

Waveform 1925 shows the output signal 1725 at node 1835 in embodiment 1800. Waveform

5 1925 corresponds to a capacitive load 1535. Waveform 1930 illustrates the output signal 1725 at  
node 1835 for a resistive-capacitive load 1535.

The embodiment 1800 (see FIG. 18) delivers a relatively constant power to load 1535.

Assume, for example, that the amplitude of the signal at node 1845 decreases as a result of a  
10 physical or environmental variation, such as rising temperature. As a result, the peak-to-peak  
amplitude at node 1830 decreases, thus implying higher current drive through PMOS transistor  
1820. As described above, however, PMOS transistor 1820 on average conducts a current equal  
to  $I$  (no DC current flows through capacitor 1705). Thus, rather than PMOS transistor 1820  
conducting an increased current in response to the voltage amplitude change at node 1830, the  
15 voltage at node 1840 decreases so as to ensure that, on average, PMOS transistor 1820 conducts  
current  $I$ . Put another way, assuming complementary operation of NMOS transistor 1815 and  
PMOS transistor 1820, the voltage at node 1840 varies in response to the physical or  
environmental change so as to ensure that PMOS transistor 1820 on average conducts current  $I$ .  
Consequently, assuming no variations in the load because of physical or environmental changes,  
20 the output buffer circuitry delivers a relatively constant power to load 1535. Thus, the output  
buffer circuitry compensates for the variations (by adjusting the voltage at node 1840) and  
delivers a relatively constant power to load 1535.

Embodiment 1800 behaves in a similar manner if the electrical characteristics of NMOS

transistor 1815 and/or PMOS transistor 1820 vary as a function of physical or environmental factors, such as process and/or temperature variations. Assume, for example, that the threshold

5 voltage ( $V_T$ ) of PMOS transistor 1820 (or NMOS transistor 1815) increases by, say, 100 mV.

Because a constant current flows on average through transistor 1820, the voltage at node 1840 will also rise by 100 mV. Consequently, the output buffer circuitry delivers a relatively constant power to load 1535.

10 FIGS. 20-23 illustrate several other embodiments according to the invention. FIG. 20

shows an embodiment 2000 of an output buffer circuitry according to the invention that can

buffer outputs of more than one VCO circuitry. Put another way, one may use the embodiment

2000 to buffer and multiplex or power down the outputs of more than one VCO circuitry. The

embodiment 2000 includes two output buffer circuitries, a first output buffer circuitry and a

15 second output buffer circuitry, that share current source 1710 and capacitor 1705. (Note,

however, that in alternative embodiments, one may split the functionality and/or circuitry of

current source 1710 and/or capacitor 1705 between the first and second output buffer circuitries,

as desired.)

20 The first output buffer circuitry in embodiment 2000 includes transistors 1815A, 1820A,

2005A, and 2010A. The first output buffer circuitry also includes biasing resistors 1825A1 and

1825A2, capacitors 1810A1 and 1810A2, inverter circuitry 2015A, current source 1710, and

capacitor 1705. Similarly, the second output buffer circuitry in embodiment 2000 includes transistors 1815B, 1820B, 2005B, and 2010B. The first output buffer circuitry also includes biasing resistors 1825B1 and 1825B2, capacitors 1810B1 and 1810B2, inverter circuitry 2015B, current source 1710, and capacitor 1705.

5

Each of the first and second output buffer circuitries essentially operates as described above in connection with FIGS. 17-18. The first and second buffer output circuitries, however, differ from the embodiments in FIGS. 17-18 in several respects.

10 First, the first and second output buffer circuitries provide a power-down or multiplex function.

Second, rather than using a single biasing resistor (such as resistor 1825 in embodiment 1800), the first and second output buffer circuitries use split biasing resistors. In other words, the first output buffer circuitry uses biasing resistors 1825A1 and 1825A2, whereas the second output buffer circuitry uses biasing resistors 1825B1 and 1825B2. The pair of biasing

15 resistors in each of the first and second output buffer circuitries (e.g., biasing resistors 1825A1 and 1825A2 in the first output buffer circuitry) perform a function similar to the function of the

biasing resistor 1825 in embodiment 1800, as described above. Third, rather than using a single coupling capacitor (such as AC-coupling capacitor 1810 in embodiment 1800), the first and second output buffer circuitries use split AC-coupling capacitors. In other words, the first output

20 buffer circuitry uses capacitors 1810A1 and 1810A2, whereas the second output buffer circuitry uses capacitors 1810B1 and 1810B2. The pair of capacitors in each of the first and second output buffer circuitries (e.g., capacitors 1810A1 and 1810A2 in the first output buffer circuitry)

perform a function similar to the function of the AC-coupling capacitor 1810 in embodiment 1800.

The power-down or multiplexing function of embodiment 2000 uses transistors 2005A,

5 2010A, 2005B, and 2010B, and inverter circuitries 2015A and 2015B. More specifically, the power-down or multiplexing function of the first output buffer circuitry in embodiment 2000 uses transistors 2005A and 2010A, and inverter circuitry 2015A. Conversely, the power-down or multiplexing function of the second output buffer circuitry in embodiment 2000 uses transistors 2005B and 2010B, and inverter circuitry 2015B. A control signal PWDN1 controls the operation  
10 of the power-down or multiplexing function of the first output buffer circuitry, whereas a control signal PWDN2 controls the operation of the power-down or multiplexing function of the second output buffer circuitry.

Control signals PWDN1 and PWDN2 may generally relate to each other depending on

15 the particular desired function. To provide a multiplexing function between the first and second output buffer circuitries, the control signal PWDN1 and PWDN2 may constitute complementary signals. To power down only one of the first and second output buffer circuitries, one may activate the corresponding power-down control signal (*i.e.*, PWDN1 or PWDN2) to that output buffer circuitry. To power down both first and second output buffer circuitries, one may activate  
20 PWDN1 and PWDN2 simultaneously. To prevent the flow of residual or leakage currents, one may turn off or power down current source 1710, as desired.

Generally, one may derive the control signals PWDN1 and PWDN2 from the power-down signal PDNB described above, as desired. In addition or instead, one may provide generalized PWDN1 and PWDN2 control signals that have an arbitrary, desired relationship to each other and/or other signals in order to realize a particular prescribed or desired power-down 5 or multiplexing functionality by the first and second output buffer circuitries.

With respect to the first output buffer circuitry in embodiment 2000, when control signal

PWDN1 has a logic-high state, transistor 2010A turns on and consequently transistor 1815A turns off. Furthermore, a logic-high state of the PWDN1 causes a logic-low output signal at the 10 output of inverter circuitry 2015A and consequently turns on transistor 2005A. The turning on of transistor 2005A causes transistor 1820A to turn off. As a result, the first output buffer circuitry becomes disabled or powered-down and does not drive the output of embodiment 2000.

Conversely, when control signal PWDN1 has a logic-low state, transistor 2010A turns

off, which allows transistor 1815A to operate in response to the output signal of the first VCO 15 circuitry ( $VCO_1$ ), as described above. A logic-low state of the control signal PWDN1 also causes a logic-high state at the output of inverter circuitry 2015A, which turns off transistor 2005A. As a result, transistor 1820A to operate in response to the output signal of the first VCO circuitry 20 ( $VCO_1$ ), as described above. Put another way, a logic low level of the control signal PWDN1 enables the output of the first output buffer circuitry.

The power-down function of the second output buffer circuitry operates in a similar manner. A logic-high state of control signal PWDN2 turns on transistor 2010B. Consequently, transistor 1815B turns off. A logic-high state of the PWDN2 also causes the output of inverter circuitry 2015B to supply a logic-low signal to transistor 2005B. In response to the logic-low signal at the output of inverter circuitry 2015B, transistor 2005B turns on. Consequently, transistor 1820B turns off. As a result, the first output buffer circuitry becomes disabled or powered-down and does not drive the output of embodiment 2000.

On the other hand, when control signal PWDN2 has a logic-low state, transistor 2010B

turns off, which allows transistor 1815B to operate in response to the output signal of the second VCO circuitry ( $VCO_2$ ), as described above. Furthermore, a logic-low state of the control signal PWDN2 also causes a logic-high state at the output of inverter circuitry 2015B. Consequently, transistor 2005B turns off, which allows transistor 1820B to respond to the output signal of the second VCO circuitry ( $VCO_2$ ), as described above. Thus, asserting a logic low level on control signal PWDN2 enables the output of the second output buffer circuitry.

Note that, although embodiment 2000 shows two output buffer circuitries, one may

generally use other numbers of output buffer circuitries, as desired. Furthermore, rather than using two power-down or multiplexing control signals, one may use other appropriate numbers of power-down or multiplexing signals. In some embodiments, the output buffer circuitries may have independent, individual power-down or multiplexing signals, whereas in other embodiments, one may derive the power-down or multiplexing signals for some of the output

buffer circuitries from a master control signal, a set of control signals, from some of the power-down or multiplexing control signals, or a combination or sub-combination of them.

The power-down or multiplexing signals for the output buffer circuitries may have an  
5 arbitrary desired relationship to one another in order to realize a prescribed or desired functionality. Moreover, note that although embodiment 2000 does not explicitly show the use of buffer circuitries 1805 (see FIG. 18), one may include buffer circuitries for each VCO output, as desired.

10 FIG. 21 illustrates an embodiment 2100 according to the invention for an output buffer circuitry that provides a differential output signal from a differential input signal. The differential input and output signals help to reduce noise and interference, as noted above. The embodiment 2100 includes first and second single-ended output buffer circuitries. The first and second output buffer circuitries may each constitute an output buffer circuitry as shown in FIG.  
15 18, although one may generally use the output buffer circuitry of FIG. 17, as desired. Together, the two single-ended output buffer circuitries receive the differential output of a VCO circuitry (not shown explicitly in FIG. 21), and produce a differential output signal.

Referring to embodiment 2100, the first and second output buffer circuitries share current  
20 source 1710 and capacitor 1705. (Note, however, that in alternative embodiments, one may split the functionality and/or circuitry of current source 1710 and/or capacitor 1705 between the first and second output buffer circuitries, as desired.) The first output buffer circuitry includes current

source 1710, capacitor 1705, capacitor 1810A, resistor 1825A, NMOS transistor 1815A, and PMOS transistor 1820A. Similarly, the second output buffer circuitry includes current source 1710, capacitor 1705, capacitor 1810B, resistor 1825B, NMOS transistor 1815B, and PMOS transistor 1820B. For each of the first and second output buffer circuitries, the MOS devices, the 5 capacitors, the resistors, and the current source perform the same or similar function as the corresponding component or device in embodiment 1800 shown in FIG. 18.

The differential output signal of the VCO circuitry (not shown explicitly) constitutes a

positive output signal and a negative output signal. The first output buffer circuitry accepts the 10 positive output signal of the VCO circuitry as its input signal. Similarly, the second output buffer circuitry receives the negative output signal of the VCO circuitry as its input signal. The first and second output buffer circuitries provide the positive and negative output signals of embodiment 2100, respectively. Together, the output signals of the first and second output buffer circuitries constitute the differential output signal of embodiment 2100.

15

Various embodiments of the invention provide added flexibility by allowing the programming of the power level of the output buffer circuitry's output signal. FIG. 22 shows an embodiment 2200 of an output buffer circuitry according to the invention that has programmable or adjustable output power level. The circuit arrangement in embodiment 2200 includes circuit 20 block 2210 and adjustable current source 2205. The circuit block 2210 includes the same devices, components, and circuit arrangement as does embodiment 1800 in FIG. 18 (or alternatively, embodiment 1700 in FIG. 17), except that the circuit block 2210 does not include

current source 1710. Thus, circuit block 2210 includes capacitor 1810 ( $C_1$ ), NMOS transistor 1815, PMOS transistor 1820, resistor 1825, and capacitor 1705 ( $C_2$ ). One may use a buffer circuitry (e.g., buffer circuitry 1805 in FIG. 18) to drive the input of embodiment 2200, as desired.

5

Rather than using current source 1710, embodiment 2200 uses adjustable current source 2205. Adjustable current source 2205 generally includes a series of  $N$  current sources, i.e., current source 2210A ( $I_1$ ), current source 2210B ( $I_2$ ), current source 2210C ( $I_3$ ), ..., and current source 2210D ( $I_N$ ). A multi-bit signal 2215 controls the operation of current sources 2210A-  
10 2210D. The multi-bit signal 2215 includes bits  $B_1$  through  $B_N$ . Each of the bits  $B_1-B_N$  controls the amount of current that a corresponding one of current sources 2210A-2210D provides. In other words, for a bit  $B_i$ , the corresponding current source conducts a current  $B_i \cdot I_i$ . If  $B_i = 0$ , then the current source generates zero current (except, for example, leakage current in a practical implementation), whereas if  $B_i = 1$ , then the corresponding current source provides current  $I_i$ .

15

The adjustable current source 2205 sums the current from each of the current sources 2210A-2210D and provides the resulting current,  $I$ , to the circuit block 2210, where

$$I = \sum_{i=1}^N B_i \cdot I_i.$$

The output power that the output buffer circuitry provides depends in part on the magnitude of current  $I$ . By providing a digital word as the multi-bit signal 2215, one may therefore adjust or program the output power level of the output buffer circuitry 2200. Note that one may use a wide variety of schemes for controlling the output power level. For example, the

user may supply the multi-bit signal 2215 a digital word through a configuration register or through baseband circuitry 120, and the like, as desired. Furthermore, control circuitry (not shown explicitly) may derive the multi-bit signal 2215 from a variety of information and parameters, such as safe-operating areas of devices within the RF circuitry, and the like, as

5 desired.

Note also that the number of the bits within the multi-bit signal line 2215,  $N$ , depends on a variety of factors that performance and design specifications and criteria for a given application may dictate or specify. For example, the number of bits,  $N$ , may depend on the desired  
10 resolution in the output power level of the output buffer circuitry. As another example, the number of bits,  $N$ , may depend on the hardware resources used to provide the digital word or considerations such as the practical number of current sources one may implement.

FIG. 23 shows an embodiment 2300 of adjustable current source 2205. Embodiment 15 2300 includes  $N$  transistors 2305A-2305D arranged as current mirrors. A current reference signal 2315 drives the gate terminals of transistors 2305A-2305D. The current that each of transistors 2305A-2305D provides depends in part on its size (e.g., its width-to-length ratio, or  $W/L$ ). One may scale transistors 2305A-2305D in any desired manner in relation to one another, thus providing a flexible scheme for providing an adjustable output current,  $I$ .

20

Embodiment 2300 also includes  $N$  transistors 2310A-2310D used essentially as switches. Each of transistors 2310A-2310D couples in series with a corresponding one of transistors

2305A-2305D (for example, transistor 2310A couples in series with transistor 2305A, and so on). If one of transistors 2310A-2310D is off, it blocks the current that the corresponding one of transistors 2305A-2305D provides. Conversely, if one of transistors 2310A-2310D is on, it conducts the current that the corresponding one of transistors 2305A-2305D provides. The 5 source terminals of transistors 2310A-2310D couple together and collectively provide current  $I$  as the output current of adjustable current source 2205. In other words, current  $I$  constitutes the sum of currents that transistors 2310A-2310D provide.

10 Multi-bit signal 2215 controls transistors 2310A-2310D. Each of the  $N$  bits in multi-bit signal 2215 controls a corresponding one of transistors 2310A-2310D. Thus, bit  $B_1$  controls transistor 2310A, bit  $B_2$  controls transistor 2310B, ..., and bit  $B_N$  controls transistor 2310D. If a 15 bit in the multi-bit signal has a logic zero value, the corresponding one of transistor 2310A-2310D turns off, and thus blocks the current provided by the corresponding one of transistors 2305A-2305D. By manipulating the bit values in multi-bit signal 2215, one may control the current that each of transistors 2310A-2310D provides and, as a result, adjust or program the output current  $I$ .

20 Note that the description of the adjustable current source 2205 in FIGS. 22-23 assumes active-low logic signals (*i.e.*, the signal within the multi-bit signal 2215 constitute active-low logic signals). One may modify the adjustable current source 2205 to adapt it to active-high logic signals by making modifications that persons of ordinary skill in the art with the benefit of the description of the invention understand.

FIG. 24 depicts a block diagram of an embodiment 2400 according to the invention.

Embodiment 2400 constitutes an output buffer circuitry with differential inputs, differential output, power down or multiplexing capability, and programmable output power level. Referring

5 to FIG. 24, embodiment 2400 includes circuit blocks 2405A and 2405B, and adjustable current

source 2205. Each of the circuit blocks 2405A and 2405B constitutes a circuit arrangement as

embodiment 2000 shown in FIG. 20, except that circuit blocks 2405A and 2405B do not contain

capacitor 1705 and current source 1710. Rather than using current source 1710 shown in FIG.

20, embodiment 2400 uses adjustable current source 2205, described above in connection with

10 FIGS. 22-23. (Note, however, that in alternative embodiments, one may split the functionality

and/or circuitry of current source 1710 and/or capacitor 1705 between the circuit blocks 2405A

and 2405B, as desired.)

Circuit block 2405A receives the positive outputs of first and second VCO circuitries

15 ( $VCO_1(P)$  and  $VCO_2(P)$ , respectively). Circuit block 2405A provides the positive output (labeled

as Output( $P$ ) in FIG. 24) of embodiment 2400. Similarly, circuit block 2405B receives the

negative outputs of first and second VCO circuitries ( $VCO_1(N)$  and  $VCO_2(N)$ , respectively).

Circuit block 2405B generates the negative output (labeled as Output( $N$ ) in FIG. 24) of

embodiment 2400. Both circuit block 2405A and circuit block 2405B use the power-down or

20 multiplexing signals PWDN1 and PWDN2 to provide the multiplexing or power-down feature

described above.

Adjustable current source 2205 provides an adjustable or programmable current  $I$  to circuit blocks 2405A and 2405B. As described above, the magnitude of current  $I$  and, hence, the power level at the differential output (*i.e.*, the output signal provided by Output( $P$ ) and Output( $N$ )) depends on the bit values within multi-bit signal 2215. One may adjust the output power level by programming the bit values, as described above. Furthermore, as described above, one may use active-low or active-high logic and/or incorporate input buffer circuitry (*e.g.*, buffer circuitry 1805 in FIG. 18), as desired. FIG. 25 provides more details of the circuit arrangement within embodiment 2400, including the details of circuit blocks 2405A and 2405B, and adjustable current source 2205.

10

One may use output buffer circuitries according to the invention in a variety of applications. Some examples include RF apparatus generally and, more particularly, RF receivers, transmitters, and transceivers. Output buffer circuitries according to the invention lend themselves to use within any application that employs LO circuitries, such as LO circuitry 222 (see FIGS. 2-8). U.S. Patent Application Serial No. 09/708,339, Attorney Docket No. SILA:035C1, titled “Method and Apparatus for Operating a PLL with a Phase Detector/Sample Hold Circuit for Synthesizing High-Frequency Signals for Wireless Communications,” filed on November 8, 2000, and incorporated by reference here, provides additional embodiments and further details of LO circuitries in which one may include one or more output buffer circuitries according to the invention.

20

FIGS. 26A-26C shows several embodiments of LO circuitries that use output buffer circuitries according to the invention. Each of FIGS. 26A-26C includes one or more PLL circuitries 2605. PLL circuitry 2605 may include a phase detector, a loop filter, and one or more VCO circuitries in a feedback loop, as persons of ordinary skill in the art understand.

5

In LO circuitry 2600A in FIG. 26A, a PLL circuitry 2605 drives the input of output buffer circuitry 2610 according to the invention. Output buffer circuitry 2610 drives an output of LO circuitry 2600A. Output buffer circuitry 2610 may constitute one of the embodiments according to the invention, as described above. Output buffer circuitry 2610 may incorporate 10 single-ended or differential input and output signals, as desired. Furthermore, output buffer circuitry 2610 may include power-down or multiplexing, and programmable and/or adjustable output power features, as desired. Note that one may use an arrangement where the LO circuitry includes a plurality of PLL circuitries 2605, each of which drives a respective input of a plurality 15 of output buffer circuitries 2600A. Each of the output buffer circuitries in turn drives a respective output of the LO circuitry.

In FIG. 26B, LO circuitry 2600B has  $K$  outputs. LO circuitry 2600B includes PLL circuitry 2605 with  $K$  outputs, and  $K$  output buffer circuitries denoted as 2610A-2610C. PLL circuitry 2605 drives the respective inputs of output buffer circuitries 2610A-2610C. Each of 20 output buffer circuitries 2610A-2610C drives a respective output of LO circuitry 2600B. Each of output buffer circuitries 2610A-2610C may constitute one of the embodiments according to the invention, as described above. One or more of output buffer circuitries 2610A-2610C may

incorporate single-ended or differential input and output signals, as desired. Furthermore, one or more of output buffer circuitries 2610A-2610C may include power-down or multiplexing, and/or programmable or adjustable output power features, as desired.

5 LO circuitry 2600C in FIG. 26C includes  $M$  PLL circuitries, denoted as 2605A-2605C, and an output buffer circuitry 2610 that has  $M$  inputs. Each of PLL circuitries 2605A-2605C drives a respective input of output buffer circuitry 2610. Output buffer circuitry 2610 drives an output of LO circuitry 2600C. Output buffer circuitry 2610 may constitute one of the embodiments according to the invention, as described above, and includes the power-down or  
10 multiplexing feature in order to multiplex a selected output of one of PLL circuitries 2605A-2605C to the output of LO circuitry 2600C. Output buffer circuitry 2610 may incorporate single-ended or differential input and output signals, as desired. Furthermore, output buffer circuitry 2610 may include programmable or adjustable output power features, as desired.

15 Note that, rather than or in addition to using the embodiments provided here, one may use many other embodiments of the various circuit blocks and arrangement of circuitry. As persons of ordinary skill in the art who have read the description of the invention will understand, one may use a variety of implementations of the invention, depending on factors such as design and performance specifications. For example, rather than using MOS switches, one may use other  
20 types of switches, as desired. Furthermore, rather than buffering the output signal of a VCO circuitry, one may generally use the inventive concepts to buffer any RF signal such that the buffer circuitry delivers a constant power to a load.

Referring to the figures, for example, FIGS. 16 and 24, the various blocks shown depict mainly the conceptual functions and signal flow. The actual circuit implementation may or may not contain separately identifiable hardware for the various functional blocks. For example, one  
5 may combine the functionality of various blocks into one circuit block, as desired. Furthermore, one may realize the functionality of a single block in several circuit blocks, as desired. The choice of circuit implementation depends on various factors, such as particular design and specifications for a given implementation, as persons of ordinary skill in the art who have read  
10 the disclosure of the invention will understand.

Further modifications and alternative embodiments of the invention will be apparent to persons skilled in the art in view of the description of the invention. Accordingly, this description teaches persons of ordinary skill in the art the manner of carrying out the invention and the embodiments described are to be construed as illustrative only.

The forms of the invention shown and described should be taken as exemplary embodiments. Persons of ordinary skill in the art may make various changes in the shape, size and arrangement of parts without departing from the scope of the invention described in this document. For example, persons skilled in the art may substitute equivalent elements for the  
15 elements illustrated and described here. Moreover, persons of ordinary skill in the art who have the benefit of the description of the invention may use certain features of the invention independently of the use of other features, without departing from the scope of the invention.